

# **A Dual-Mode Q-enhanced RF Front-End Filter for 5 GHz WLAN and UWB with NB Interference Rejection**

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by

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# ABSTRACT

The 5 GHz Wireless LAN (802.11a) is a popular standard for wireless indoor communications providing moderate range and speed. Combined with the emerging ultra Wideband standard (UWB) for short range and high speed communications, the two standards promise to fulfil all areas of wireless application needs. However, due to the overlapping of the two spectrums, the stronger 802.11a signals tend to interfere causing degradation to the UWB receiver. This presents one of the main technical challenges preventing the wide acceptance of UWB.

The research work presented in this thesis is to propose a low cost RF receiver front-end filter topology that would resolve the narrowband (NB) interference to UWB receiver while being operable in both 802.11a mode and UWB mode. The goal of the dual mode filter design is to reduce cost and complexity by developing a fully integrated front-end filter. The filter design utilizes high Q passive devices and Q-enhancement technique to provide front-end channel-selection in NB mode and NB interference rejection in UWB mode.

In the 802.11a NB mode, the filter has a tunable gain of 4 dB to 25 dB, NF of 8 dB and an IIP3 between -47 dBm and -18 dBm. The input impedance is matched at -16 dB. The frequency of operation can be tuned from 5.15 GHz to 5.35 GHz. In the UWB mode, the filter has a gain of 0 dB to 8 dB across 3.1 GHz to 9 GHz. The filter can reject the NB interference between 5.15 GHz to 5.35 GHz at up to 60 dB. The Q of the filter is tunable up to a 250 while consuming a maximum of 23.4 mW of power. The fully integrated dual mode filter occupies a die area of 1.1  $mm^2$ .

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## List of Abbreviations

BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
dB	decibel
dBm	decibel with reference to 1mW of power
FCC	Federal Communications Commission
Hz	Unit of measurement for frequency
IC	Integrated Circuit
LC	Parallel inductor and capacitor resonator
LNA	Low Noise Amplifier
MOS	Metal Oxide Semiconductor
MOSCAP	Metal Oxide Semiconductor Capacitor
NB	Narrowband
NBI	Narrowband Interference
nMOS	n-channel MOS
PCB	Printed Circuit Board
PGS	Patterned Ground Shield
pMOS	p-channel MOS
Q	Quality Factor
RF	Radio Frequency
Si	Silicon
SNR	Signal to Noise Ratio
SRF	Self Resonating Frequency
TFB	Test Fixture Board
UWB	Ultrawideband
VCO	Voltage Control Oscillator
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

# 1. Introduction

## 1.1 RF Front-End Filter

Research in low cost designs and fabrications of RFIC receivers is everlasting. In the design front, researchers focus on reducing cost and complexity by moving towards a fully integrated monolithic receiver design. One of the most challenging blocks to integrate in the receiver is the RF front-end filter. High performance requirements such as high linearity, high quality factor (Q) and low noise figure at the front-end makes the filter challenging to implement monolithically. Most commercial RF receivers today use off-chip surface acoustic wave (SAW) filter for pre-filtering, while channel-selection is achieved in the receiver back-end. The use of off-chip components adds to the overall cost of the receiver and results in a bulky receiver design. Signals traveling off-chip need to drive large capacitances that are associated with the printed circuit board (PCB). The requirements of input and output matching circuits also add complexity and increases power. Hence, the realization of monolithic front-end filter is important in a low cost receiver design.

### 1.1.1 Integrated RF Filter Performance

The objective of the front-end filter is to receive and process the intended signal while rejecting all other interferences. The integrity of the signal is passed on to the other blocks in the receiver for further processing. As a result, the filter is required to have good performance as it has the most effect on the overall performance of a receiver. For low noise and low power requirement, most integrated RF filters are

based on parallel inductor and capacitor (LC) resonator topologies. However, these topologies exhibit poor performance because of the low quality factors of on-chip inductors. The effect of low Q means channel selection and interference rejection from nearby channels are difficult.

The important performance criteria for a receiver is noise figure and linearity, both of which determine the range of signal powers it can receive. Filter selectivity is also important for channel-selection and interference rejection. The following are main the specifications that are used to determine the performance of a filter.

### Noise Figure

The lowest signal level that a receiver can detect is called the receiver's sensitivity. It is determined by the thermal noise floor in the environment along with the receiver's noise figure (NF) which is defined as the ratio of how much the signal-to-noise ratio (SNR) of the signal is degraded as it passes through the receiver.

$$NF = \frac{SNR_{in}}{SNR_{out}} \quad (1.1)$$

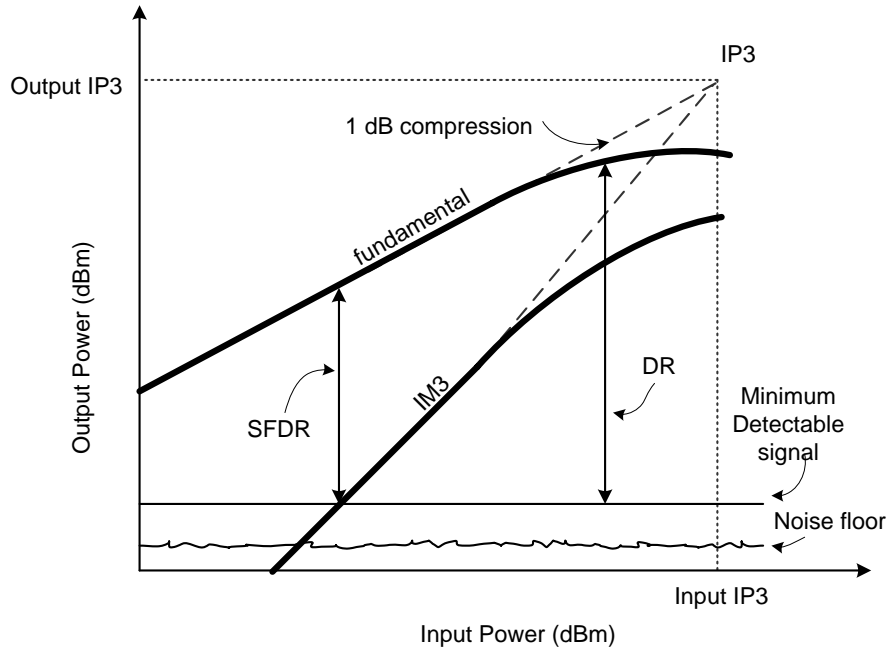
The overall noise figure of a receiver is given by Friis equation below to account for the power gain (G) contribution of each stage [1]. The equation indicates that the noise contribution of each stage decreases as the gain in the preceding stage increases. Thus, a low noise amplifier with high gain is often desired in the first stage in a receiver.

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{G_1} + \dots + \frac{NF_m - 1}{G_1 \dots G_{m-1}} \quad (1.2)$$

### Linearity

All devices in an RF circuit exert nonlinearity which causes the output signal to become distorted. The distortion determines the maximum receivable input power for the receiver. The linearity of an RF circuit is commonly described by the 1-dB

compression point or the third-order intercept point (IP3). The 1-dB compression point is defined as the input signal level that causes the gain to decrease by 1 dB. Two signals that are offset by some frequency can intermodulate causing distortion. The IP3 measures the theoretical point where the intermodulation tones are equal to the amplitudes of the fundamental tones. The location of the 1-dB and the IP3 compression points plot are shown on Figure 1.1.



**Figure 1.1** Noise and Linearity Graph for Input/Output Power

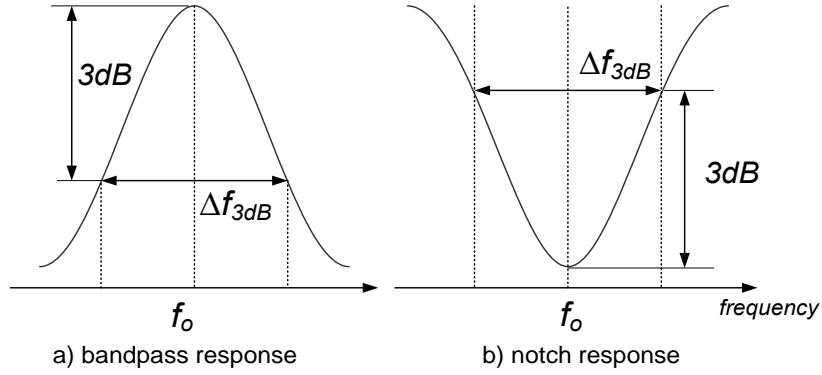
## Dynamic Range

The range of input signal level at which the receiver can accommodate while producing an acceptable signal quality is defined as the dynamic range. As shown in Figure 1.1, the spurious-free dynamic range (SFDR) is defined as the maximum input level in which the third-order intermodulation products do not exceed the noise floor. The dynamic range (DR) is defined as the minimum detectable signal to the 1dB compression point.

## Selectivity

Signals from neighboring channels and other sources close to the intended signal can interfere causing distortion. The receiver's ability to select and process the signal at the presence of interference is called the receiver's selectivity. The RF block in the receiver responsible for selectivity is the channel-select filter block. Selectivity is quantized using the concept of quality factor,  $Q$ , which measures the sharpness of the filter response. Hence, higher  $Q$  equals higher selectivity. Mathematically,  $Q$  is defined as the filter's frequency of operation over the 3 dB bandwidth frequency as stated in Equation 1.3. The 3 dB point is referenced from the peak or depth of the filter response as shown in Figure 1.2.

$$Q_{3dB} = \frac{f_o}{\Delta f_{3dB}} \quad (1.3)$$



**Figure 1.2** Definition of Filter Quality for a) Bandpass b) Notch Response

## 1.2 Multiple Standards Receiver

The cost of the receiver can be further reduced by designing a receiver that is compatible with multiple standards. This versatile capability allows a receiver to

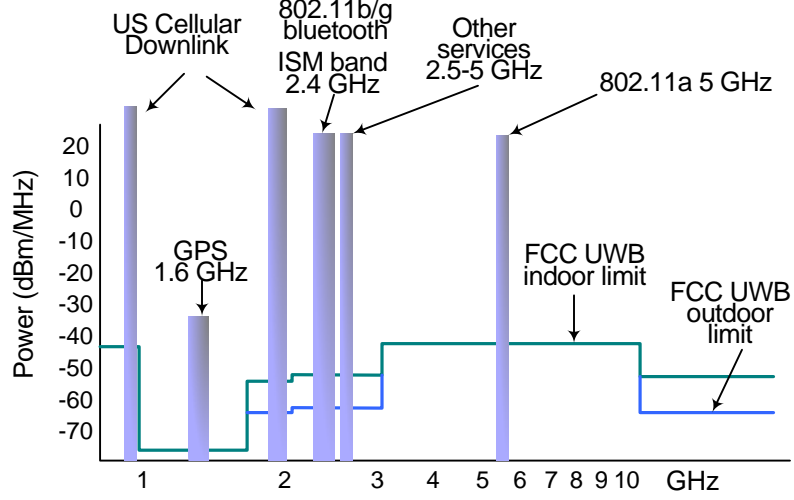
support various wireless applications in a single device adding more functionality and market competitiveness. In the area of personal wireless communications, the two most popular standards today are the 5 GHz Wireless Local Area Network (WLAN) and the emerging Ultra Wideband (UWB). Implementing a low cost receiver that supports both the UWB and NB (narrowband) standards will bring in a new wave of wireless applications in the personal wireless communications market. The challenge that first needs to be resolved is to eliminate the NB interference on the UWB receiver to allow the two standards to seamlessly co-exist in the same environment.

### 1.3 UWB and NB Co-Existence

The Ultrawideband (UWB) spectrum was approved by the Federal Communication Commission (FCC) on February 14, 2002 for indoor short range communications. This 7.5 GHz of ultrawide bandwidth opens up the possibility of a cable-free high speed wireless network in a home or office environment. FCC ruling places limitations on UWB to ensure interference to existing spectrums is minimal, while not restricting its capabilities and benefits. As a result, indoor UWB signals are restricted to 3.1 GHz to 10.6 GHz and can emit no more than -41.3 dBm/MHz of power. This level of emission is comparable to what is allowed for the unintentional radio frequency energy radiated today by electronic devices such as computers. UWB communication is ideal for indoor high speed short range data transmissions of up to tens of meters. The wide UWB bandwidth means that it also overlaps with the same spectrum as the 802.11a WLAN, as seen in Figure 1.3.

To be defined as UWB, the signals must have either a fractional bandwidth greater than 20%, or a bandwidth that is more than 500 MHz, whichever is less [2]. The loose definition of UWB signals means that UWB is a versatile spectrum that can accommodate multiple independent wireless standards. This flexibility, however, has given rise to many competing proposals for the UWB standard such as DS-UWB and





**Figure 1.3** Spectrum Allocation of UWB

Multiband OFDM [3, 4].

NB 802.11a operates in three distinct 100 MHz regions with different power limitations in the 5 GHz bands. The lower band ranges from 5.15 - 5.25 GHz and has a power limitation of -3.01 dBm/MHz. The mid band is from 5.25 - 5.35 GHz and is limited by 3.98 dBm/MHz. The upper band is from 5.725 - 5.825 GHz and is limited at 10 dBm/MHz. In the United States, FCC has allocated all 3 bands for unlicensed usage. While in Europe, only low and mid bands are unlicensed and in Japan, only the low band is available. Only the lower and mid band is of concern as both co-exist with the UWB in the indoor environment. Soon after the UWB standard was approved, it was realized that the interference from the existing NB service, specifically the 802.11a, presented a problem for the UWB receiver as both spectrums co-exist in the same environment and overlaps at 5 GHz. As the 802.11a signals are much stronger, they can block the desired signal causing the receiver to be desensitized. The interference is significant since the 802.11a signals are drastically higher at -3 dBm/MHz in the lower band to 10 dBm/MHz in the upper band. Studies have shown that the harmful effects include receiver overloading and desensitivity. The

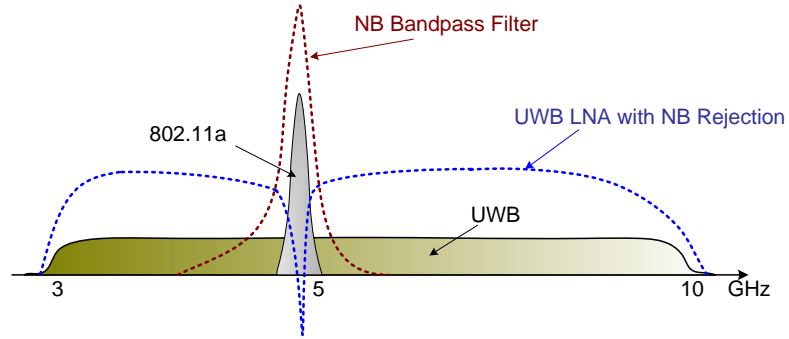
magnitude of the effect depends on the probability of the signals overlapping and the relative distance between the two sources from the UWB receiver. The NB signals can cause significant interference to the UWB reception and degradation of the attainable throughput of the UWB system [5, 6]. This is one of the main technical challenges that have slowed down the wide adoption of UWB into wireless applications.

## 1.4 Motivation and Contributions

Many areas of research dealing with the NB interference to UWB systems issue have been investigated in recent years [7, 8, 9]. In [7], a receiver architecture is proposed that employs frequency conversion to isolate and filter the WLAN interference. Although the method is effective, it also reduces the usable UWB bandwidth to 2.7 GHz. In [8], the author designed a tunable LNA (low noise amplifier) that operates from 6 to 10 GHz, completely avoiding the 5 GHz interference. By avoiding the interference, however, the usable UWB bandwidth is reduced to only 4 GHz. Resolving the NB interference at the RF front-end of the UWB receiver by using a notch filter is another solution. Conventional notch filters are not versatile, however, as they have a fixed notch frequency and bandwidth and cannot be turned off if required. In [9], the authors use a stripline filter to provide frequency tunable notching at 5 GHz. The addition of the passive UWB filter with WLAN notching in the RF front-end adds to the overall noise figure and receiver complexity. Previous solutions to NB interference above limits the potential of the UWB spectrum which is to offer a wide bandwidth resulting in high speed, low cost receiver architecture.

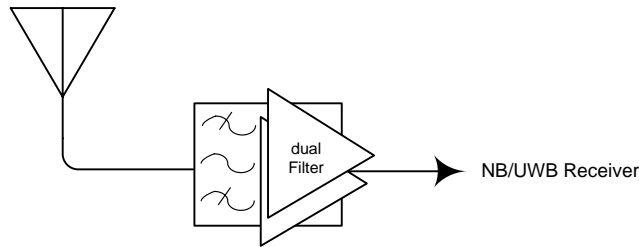
This thesis work covers the study of integrated passive devices for design and performance optimization applicable to RFIC circuits, particularly focusing in the area of RF front-end filter design. Q-enhancement filtering technique is adapted to develop a low cost filter with channel selection and interference rejection capabilities.

In addition to making the UWB receiver robust to 5 GHz WLAN interference, further motivation for the research is to take advantage of the co-existence of the 5 GHz and UWB services and design an RF front-end filter that can support both standards. Wireless devices can benefit if 5 GHz and UWB services can work together to provide interoperativity. For example, instead of designing a wireless devices that is either compatible with a UWB Personal Area Network (PAN) or the 5 GHz WLAN, a dual mode wireless device can provide more functionality by communicating with both networks. The dual mode filter concept is shown in Figure 1.4. The filter is to be the



**Figure 1.4** Proposed Dual Mode RF Front-End Characteristics

first RF block in the receiver as shown in Figure 1.5. In the absence of interference, the



**Figure 1.5** RF Front-end Proposed Dual Filter

filter functions as a wideband LNA without the interference rejection, thus, saving power for UWB receiver. This design brings in the possibility of a dual standard 802.11a and UWB receiver to be realized in a single chip. This will be a low cost

solution since it would eliminate many similar front-end components such as preselect filter, notch filter and LNA.

## 1.5 Thesis Outline

The thesis work begins with a study of integrated passive devices as they are essential for the design of low power, low cost and high frequency RFIC circuits. Chapter 2 looks at the design and optimization techniques for the resistor, capacitor, varactor, inductor and transformer. Chapter 3 introduces the concept of Q-enhancement compensation and active gain to realize a fully monolithic Q-enhanced filter. Since the filter is to be used at the RF front-end, narrowband and wideband frequency matching techniques are covered. This will then lead into Chapter 4 where a design of a proposed dual mode filter is presented. The objective of which is to provide further RFIC integration and robustness to NB interference while providing future wireless applications to utilize both modes - the 802.11a for wide range WLAN and UWB for high speed PAN. This is followed by the conclusion and suggestions for future work in Chapter 5.

## 2. Integrated Passive Devices

The resistor, capacitor, varactor, inductor and transformer are necessary passive devices for the realization of RF circuits. Monolithic devices, however, suffer from excessive parasitic capacitances and resistances resulting in a low quality factor ( $Q$ ) affecting the performance of RF circuits.  $Q$  is defined as the ratio of the reactive divided by the resistance of a device as shown in Equation 2.1.

$$Q = \frac{|Im(Z)|}{|Re(Z)|} \quad (2.1)$$

Although the integration of the resistor, capacitor and varactor have been done for quite some time, better processes and research has lead to improved performance. Because of the complexity of inductor and transformer behavior, only recently has research made realizing of monolithic inductor and transformer possible. This is partly contributed to advanced models that accurately predicts the characteristics at high frequencies. In this chapter, integrated passive device issues, concept and design examples used in this research work are presented.

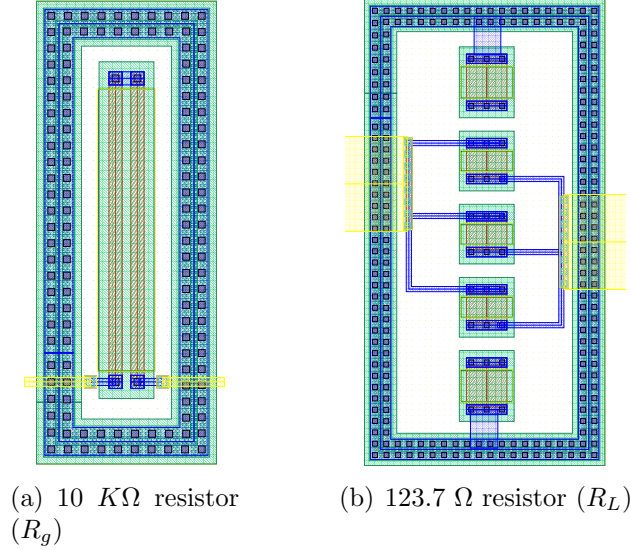
### 2.1 Resistor

Polysilicon resistors are the most popular type of resistor available in a polysilicon-gate CMOS process due to its high resistance per area [10]. The structure is made using a strip of poly deposited on top of field oxide exhibiting a sheet resistance,  $R_s$ , of 20 to 30 ohms/square. By making the width thin, a substantial large resistance

per area is realized without increase in mismatch as shown in Equation 2.2.

$$R = R_s \frac{L}{W} \quad (2.2)$$

A standard layout of a  $10\text{ K}\Omega$  polysilicon resistor is shown in Figure 2.1(a). The resistor is separated by two segments each having a length of  $8.3\mu\text{m}$  and a minimum width  $0.18\mu\text{m}$ . Guard ring, created from p+ implant, is placed around the device to reduce substrate noise which are caused by adjacent circuits injecting current into one another [11]. The simple resistor layout in Figure 2.1(a) is sensitive to process variation resulting variation as much as 20% making it useful as an RF blocker. Figure



**Figure 2.1** (a) Layout of a Simple  $10\text{K}\Omega$  Resistor (b) Layout of a Matched  $123.7\text{ }\Omega$  Resistor

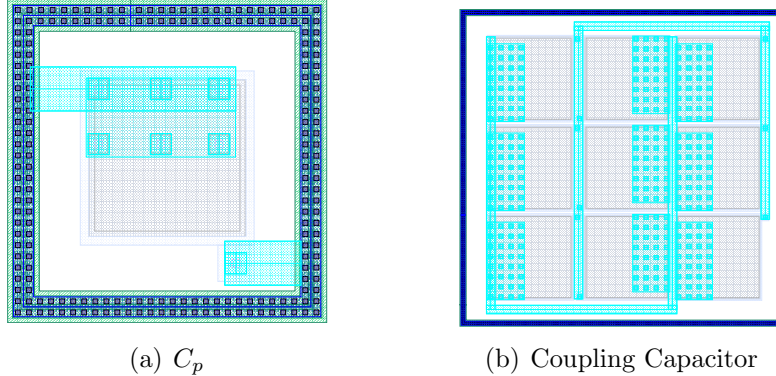
2.1(b) shows a resistor layout that is suitable for use in a voltage biasing circuit or as a resistor load as it offers improved tolerance against process variations. The layout contains five resistors each with length of  $1.5\text{ }\mu\text{m}$  and a width of  $1.8\text{ }\mu\text{m}$  obtaining a value of  $371\text{ }\Omega$ . The larger width makes the resistor less susceptible to variation. Three unit resistors connected in parallel realizes a resistance of  $123.7\text{ }\Omega$ . The layout reduces the variation by a factor of 3 since the resistors are connected in parallel.

Dummy resistors are added to ensure the three unit resistors see the same adjacent structures improving device matching. The dummy is grounded to reduce noise from coupling to the resistor.

## 2.2 Capacitor

A capacitor can be made from any of the metal layers in a process. To reduce die area, metal-insulator-metal (MIM) capacitor is a popular choice. MIM capacitor is made from special dual metal layers containing a thin oxide resulting in the highest capacitance per area available in a CMOS process.

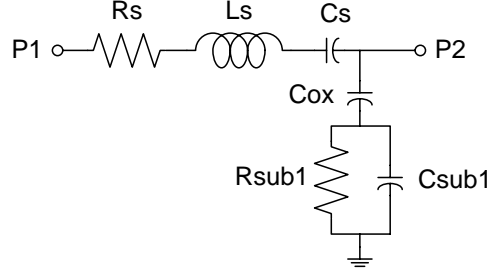
A layout of two MIM capacitors used for different application in an RF circuit is shown in Figure 2.2. A small 263.2 fF capacitor with a dimension of  $16.3 \mu m$  by  $16.3 \mu m$  is shown in Figure 2.2(a). A large capacitor is implemented using multiple unit capacitors to allow for the capacitor to be matched making it less sensitive to process variation. Figure 2.2(b) shows a coupling capacitor laid out using multiple unit cells. A unit cell valued of 410.8 fF was connected in parallel of 9 blocks to realize a 3.70 pF. Each cell unit is  $20 \mu m^2$  and the total area is  $68.9 \mu m^2$ . When modeling the



**Figure 2.2** a)  $C_p$  263.3 fF Capacitor b) A 3.70 pF Coupling Capacitor

MIM capacitor, substrate effect must also be accounted for. The MIM capacitor can be modeled with the equivalent circuit shown in Figure 2.3. The series capacitor,  $C_s$ ,

represents the inter-metal dielectric capacitance.  $R_s$  and  $L_s$  account for the parasitics existing in the electrodes.  $C_{ox}$ ,  $C_{sub1}$  and  $R_{sub1}$  are parasitics that represent the capacitance and resistance to ground due to the bottom plate metal.



**Figure 2.3** MIM Capacitor Equivalent Circuit

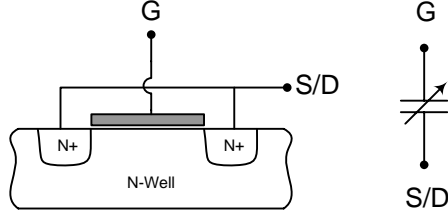
## 2.3 MOS Varactor

A varactor is essential for RF applications to operate over a range of frequencies and also to accommodate process variations. It is widely used as part of the parallel LC resonator in RF applications to alter the operating frequency of the filter. Varactors are designed to achieve high  $Q$ , sufficient capacitive tuning ratio, low parasitic capacitance, high capacitance-to-area ratio and a capacitive tuning curve that is constant and predictable [12].

Today, the varactor is commonly implemented using a MOSFET device with the source and drain connected at the same node. The gate capacitance varies as the gate bias varies from well below to well above the threshold voltage. The most common MOSFET varactor is the accumulated-mode MOS varactor as shown in Figure 2.4. The accumulated-mode device is similar to an NMOS device except it is fabricated in an n-well instead of the normal p-substrate. Accumulation-mode varactor has the advantage of a linear capacitance tuning curve and high  $Q$ . The value of  $Q$  in the range of one hundreds was reported in [12] due to the higher carrier mobility in the

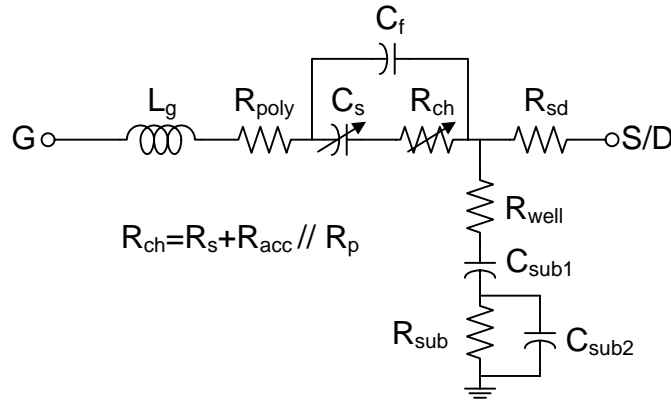


n-well. Recent researches [12, 13, 14, 15] show that accumulation-mode MOSFET-based varactors offers better performance benefiting from shrinking technology size as its tuning range is directly dependent on the oxide thickness of the process.



**Figure 2.4** Accumulated-Mode MOS Varactor

Accurate modeling of varactor is a challenge because of the structure's strong dependency on process parameters. Theoretical and SPICE compatible models do not accurately predict the quality factor-voltage (Q-V) curve since the series resistance is modeled as a constant value. Accurate modeling requires that the bias dependent of the series resistance,  $R_{ch}$ , be included in the model [16]. One such model based on semi-empirical equations is shown in Figure 2.5 [17]. In this model,  $C_s$  represents the



**Figure 2.5** A Scalable Equivalent Circuit of an Accumulation-Mode MOS Varactor

series connections of the gate oxide capacitance and the depletion region in the silicon under the gate oxide.  $C_f$  represents the fringing capacitance mainly associated with

the sidewall of the gate.  $L_g$  and  $R_{poly}$  are the parasitic inductance and distributed resistance of the gate electrode. The gate bias dependence of the channel resistance  $R_{ch}$ ,  $R_{acc}$ ,  $R_p$ , and  $R_s$  are also included.  $R_{acc}$  represents the resistance of the accumulation layer formed in the channel region.  $R_p$  is the n-well resistance in parallel with  $R_{acc}$  and  $R_s$  is the gate bias independent resistance of  $R_{ch}$  in series with the parallel connections of  $R_{acc}$  and  $R_p$ .

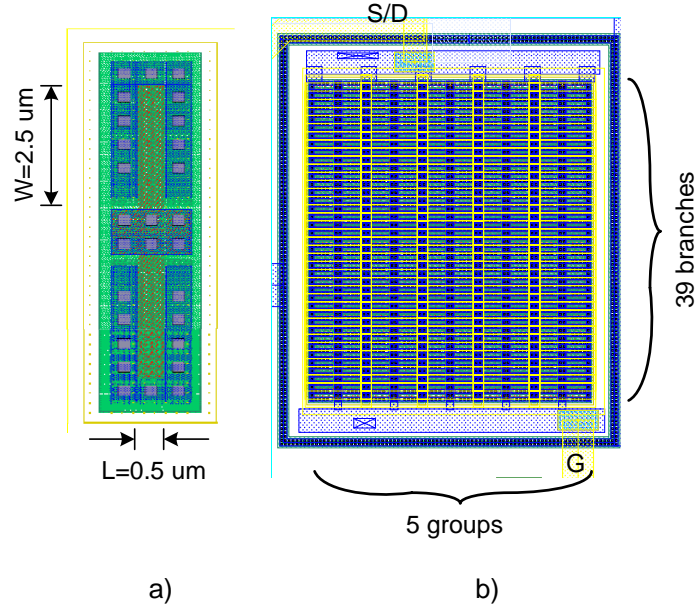
### 2.3.1 MOS Varactor Design

The Q of the varactor is mainly limited by the resistances in the gate and channel. To reduce gate resistance and area, MOS varactor's are implemented with multiple fingers. Since the parasitic resistance scales with the channel length, small length is used to increase Q. But if length is too small, the channel length resistance will dominate [17] decreasing Q. Figure 2.6 shows a design of an accumulated-mode varactor implemented in an array. Each unit pair has a gate length of  $0.5 \mu m$  and a unit width of  $2.5 \mu m$ . A branch of 39 by 5 groups were used to obtain the varactor with a nominal capacitance of 3.33 pF.

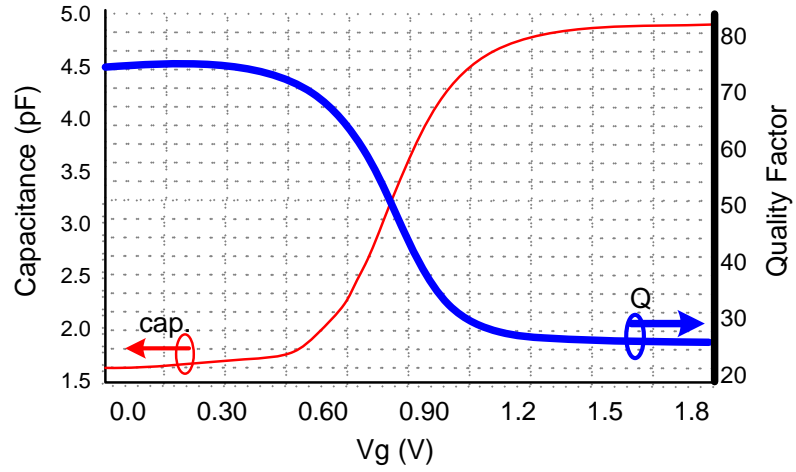
The characteristic of the varactor is obtained in Figure 2.7 where S/D is connected to 1.8V and the gate voltage is swept from 0V to 1.8V. The varactor has a maximum capacitance of 4.9 pF at 1.8V and a minimum of 1.77 pF at 0 V gate voltage. A capacitance ratio of 2.77 and a tuning range of 147% was achieved. The device layout was extracted to find the actual Q taken into account of parasitic capacitance and contact and line resistance. The Q of the varactor ranges from 75 and decreases to 26 as capacitance is increased when simulated at 5 GHz.

## 2.4 Inductor

Monolithic inductor is an important device governing the performance of many RFIC circuits. It is essential for the design of low cost, low power supply, high



**Figure 2.6** a) A MOSCAP Cell b) MOSCAP Array

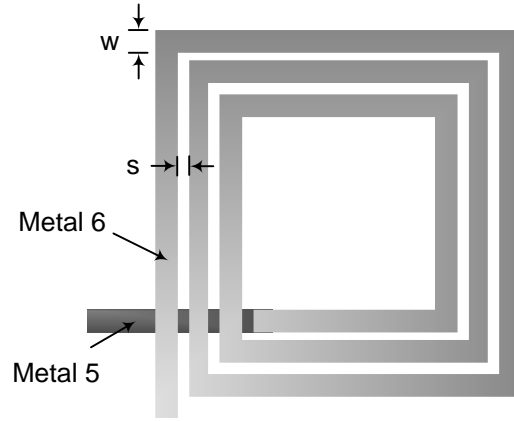


**Figure 2.7** Accumulation-Mode Varactor Capacitance and Q Curves

operating frequency, low noise levels and high level of integration in a receiver [18].

Monolithic inductor is created by winding a low sheet resistance metal line into a spiral on a planar surface. The top most layer is often used for the metal line as it is the thickest layer with lowest sheet resistance furthest from the substrate, reducing

capacitance coupling to the substrate. In a 6-metal process, the top layer (metal 6) is interwound to realize an inductor. Metal 5 layer is used to provides the exit from the inner side of the spiral as shown in Figure 2.8. The physical characteristics of the inductor are the outer dimension, metal width (w), spacing (s) between adjacent turns and the number of turns (n) in the spiral.



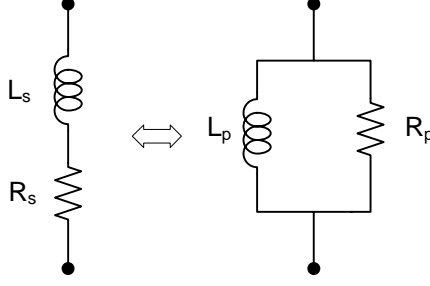
**Figure 2.8** Monolithic Square Planar Spiral Inductor

For simple analysis, the integrated inductor can be modeled simply as an inductor with a series resistor,  $R_s$ , as shown in Figure 2.9. The Q for the inductor is given in Equation 2.3. Equivalently, the inductor can be represented using a parallel model with  $L_p$  and  $R_p$ . The Q of the inductor for the parallel model is given in Equation 2.4. As will be seen in later chapters, representation of the resistance in parallel is useful for developing the Q-enhanced resonator concept.

$$Q_s = \frac{\omega L}{R_s} \quad (2.3)$$

$$Q_p = \frac{R_p}{\omega L} \quad (2.4)$$

The relationship between the series and parallel models can be seen from below. Given the impedance,  $Z_s$ , for the inductor,  $L_s$  and resistor,  $R_s$  in series, the equivalent



**Figure 2.9** A Lossy Inductor a) Series Resistance b) Equivalent Parallel Resistance

parallel inductor,  $L_p$ , and resistor,  $R_p$  impedance are found.

$$Z_s = R_s + j\omega L_s \quad (2.5)$$

$$Y_s = \frac{1}{Z_s} = \frac{R_s - j\omega L_s}{R_s^2 + \omega^2 L_s^2} \quad (2.6)$$

The inverse of the real part of  $Y_s$  gives the equivalent resistance,  $R_p$ ,

$$R_p = \frac{1}{\text{Real}(Y_s)} = \frac{R_s^2 + \omega^2 L_s^2}{R_s} = R_s \left( 1 + \frac{\omega^2 L_s^2}{R_s^2} \right) = R_s(1 + Q^2) \quad (2.7)$$

The inverse of the imaginary part of  $Y_s$  gives the equivalent inductance,  $L_p$ ,

$$L_p = \frac{1}{\text{Im}(Y_s)} = \frac{R_s^2 + \omega^2 L_s^2}{\omega^2 L_s} = L_s \left( \frac{R_s^2 + \omega^2 L_s^2}{\omega^2 L_s^2} \right) = L_s \left( \frac{Q^2 + 1}{Q^2} \right) \quad (2.8)$$

The calculations above show(s) that the series and parallel inductor models are related by its  $Q$ . For high  $Q$ ,  $L_p$  is approximately equal to  $L_s$ .

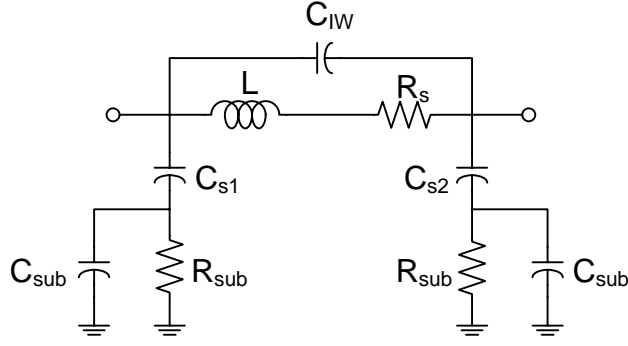
### 2.4.1 Inductor Physical Properties

Monolithic inductor suffers from low substrate resistivity of the Si-substrate contributing to low  $Q$  in the range of 6 to 10 for most commercial IC processes [19]. At low frequencies, the series resistance of inductor turns dominates the loss of the inductor. At higher frequencies, the loss is dominated by the eddy currents, which

decreases the effective area for current flow and increases the heat dissipation losses. Physical inductor has parasitic capacitances due to the coupling between windings and coupling to the substrate. The capacitance will resonate with the inductance of the inductor at a certain high frequency. The frequency at which resonating occurs is called the self resonating frequency (SRF) of the inductor. At frequencies above this point, the inductor will no longer have any inductance and will appear capacitance due to the dominance of the parasitic capacitances. Therefore, the SRF determines the upper limit for how high of frequency an inductor can operate. The SRF and Q of an inductor are highly dependent on the metal layer and layout geometry of the inductor in a process. Optimal physical geometry of an inductor is dependent on the applications and intended frequency of operation.

In the past, monolithic inductor is uncommonly found in RFIC circuits, as it requires complex 3-D simulations to precisely describe the behavior at RF and microwave frequencies. Long simulations and huge processing speed and memory size were required making it difficult to integrate into the design flow. Researches [19, 20] in the last decade resulted in simple compact models that precisely predict the behavior of the inductor minimizing the requirements for complex 3-D simulations. In addition, the use of device models provide designers the flexibility to optimize and characterize the inductor for any given RF application.

A model of an inductor with substrate effect is shown in Figure 2.10. The model does not consider frequency-dependent resistance caused by the eddy current and skin effect which limits the accuracy to a narrowband frequency range. The metal series resistance,  $R_s$  represents the eddy current effect at high frequency. Whereas  $C_{s1}$  and  $C_{s2}$  series capacitance represent the overlaps between the spiral and the connection underpass. Interwinding capacitance between inductor traces is modeled by  $C_{IW}$ .  $R_{sub}$  and  $C_{sub}$  represents the ohmic losses in the conductive substrate and metal-to-substrate capacitance, respectively.



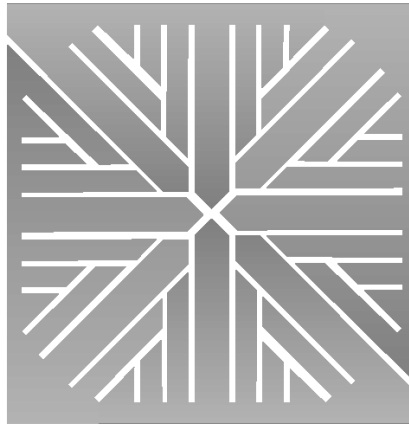
**Figure 2.10** A Narrowband Model of the Inductor

### 2.4.2 Inductor Optimization

Inductor resistivity is contributed by several factors. The active resistance of the inductor is caused by the sheet resistance of the metal line. To reduce resistivity, the thickest metal layer in the process should be used for interwinding. A wide metal strip width can decrease the spiral resistance, however, skin effect at high frequency increases if the width is made too wide. Spacing between metal turns should be as small as allowable in a process to increase the magnetic coupling between the windings to obtain higher inductance [18]. Conversely, large spacing between windings decreases magnetic coupling and increases spiral resistance and area. A large outer diameter will increase parasitic capacitance between the spiral and substrate due to increase in chip area and results in the inductor having a low SRF. The use of circular spiral geometry design allows for improved Q as it reduces the spiral resistance, but is difficult to model and fabricate accurately. A compromise is to use a 45 degree octagonal shape geometry. Inner shape of the spiral should be left hollow as it has a higher resistivity than the outer turns at high frequencies due to eddy currents, while contributing little inductance [21, 19].

The distance of the metal layer to the substrate defines the capacitance between the spiral and substrate. To minimize capacitance increasing the SRF, inductors are implemented on the top most layer. Losses in the inductor is also caused by the flow

of small signal current from the inductor to the substrate through capacitive coupling and induced through magnetic coupling. A simple technique to minimize the loss is to place a patterned ground shield (PGS) between the inductor and the substrate as shown in Figure 2.11. Metal ground shield can be used to eliminate the silicon parasitics associated with the bottom plate of the capacitors. The metal shield is patterned with slots orthogonal to the spiral to prevent the flow of image current, also known as loop current, which is caused by the magnetic field of the spiral. This loop current reduces the magnetic field in the inductor resulting in a loss of the overall inductance [22]. To prevent the loop current from flowing along the outer edge of the plane, the PGS is created from two separate metal planes.



**Figure 2.11** A Patterned Ground Shield

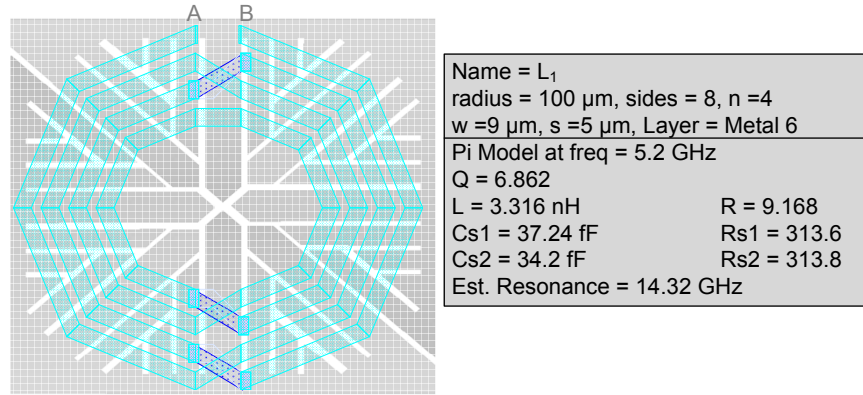
### 2.4.3 Various Inductor Designs

Integrated inductor optimization is a tedious and time consuming task, but can be aided by a tool called ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for ICs) [23]. ASITIC assists the designer with inductor structural optimization by solving Maxwell's equations saving designers a great amount of time. The techniques are fairly accurate, taking into account substrate coupling, current



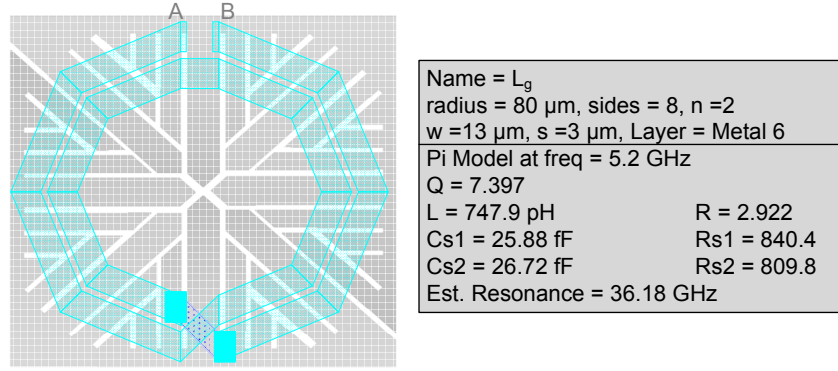
constriction, and proximity effects. The analysis is also fast and efficient, making it suitable for computer optimization.

The following figures show various inductor layouts, optimized for applications at 5 GHz and operable above 10.6 GHz. Figure 2.12 shows a 3.316 nH octagonal shape inductor, implemented on metal-6 with PGS, with a Q of 6.862. Large number of turns are required to obtain the large inductance. The addition of the PGS reduces the substrate resistance, Rs1 and Rs2, but increases the substrate capacitance, Cs1 and Cs2 resulting in the SRF of 14.32 GHz. Figure 2.13 shows a layout of a smaller

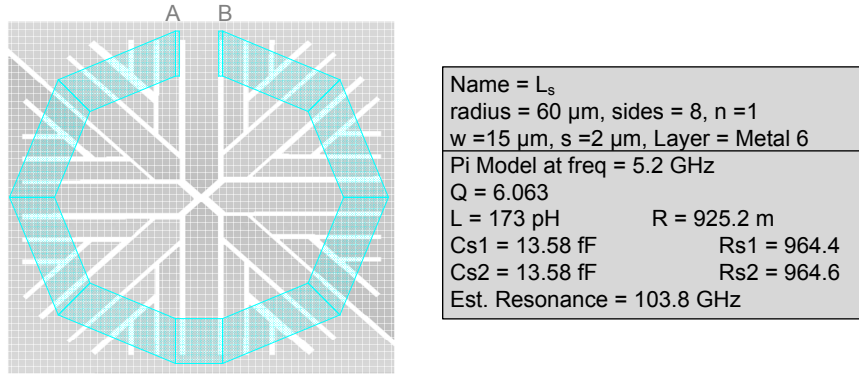


**Figure 2.12** A 3.316 nH Inductor with PGS

inductor with a value of 747.9 pH. The structure has a smaller inductance due to a smaller number of turns of two. Hence, parasitic capacitance are reduced resulting in a high SRF of 36.18 GHz. Larger width in this design also aided to obtain a Q of 7.393. Figure 2.14 shows a single turn inductor realizing a small inductance of 173 pH. Width is made larger to reduce the metal resistance, but Q is slightly lower at 6.063 since inductance is also reduced. The SRF is high since the structure is smaller, with a radius of only 60  $\mu$ m. In the previous three inductor designs, the inductors were optimized mainly for high Q, with very little regard to area. However, as it will be shown, inductor can be purposely designed for low Q to reduce component count and die area. For wideband RF application, inductor and series resistance load is

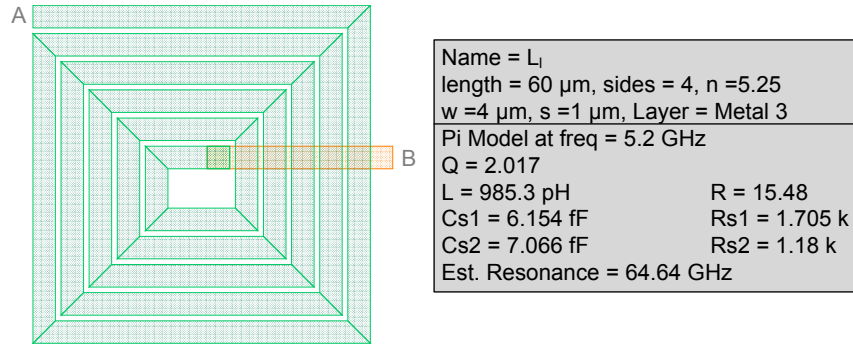


**Figure 2.13** A 747.9 pH Inductor with PGS



**Figure 2.14** A 173 pH Inductor with PGS

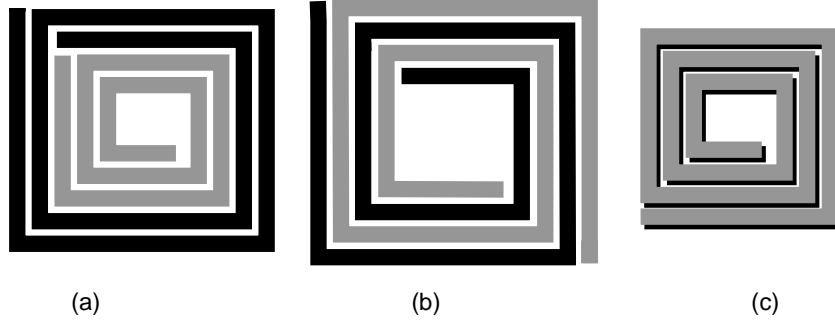
used to achieve a flat gain throughout the bandwidth. Scarce die area can be saved by incorporating the series resistance in the design as part of the parasitic resistance of the inductor. This means that the inductor does not need to have high  $Q$ , hence, it can be designed purposely to obtain the low  $Q$  necessary to account for the series resistance eliminating the need of a resistor. Shown in Figure 2.15, the 985.3 pH inductor has a  $Q$  of only 2.017 and a length of  $60\text{ }\mu\text{m}$ . The inductor was laid out using an un-optimized square structure. The inductor turns was increased to 5.25 to improve the inductance value. High resistance metal 3 layer was used to create the metal strip. PGS was not included resulting in a series resistance increase of 15.48  $\Omega$ .



**Figure 2.15** A 983.2 pH Inductor

## 2.5 Transformer

Transformers are used in RFIC applications in place of two inductors in differential circuits to obtain higher Q while occupying less die area. They are also used for single to differential signal conversion, impedance matching, signal coupling and phase splitting [24]. A transformer is created when two spiral windings, or inductors, magnetically couple due to their close proximity. This causes the impedance levels, defined as the ratio of the terminal voltage to the current flow, to change between windings [25]. The transformer characteristics include the self-inductance, series resistance, mutual coupling coefficient, substrate capacitances, self resonating frequencies, symmetry and die area. Similar to inductor, the type of transformer structure influences these characteristics and is selected based on the application usage the transformer is intended for. The three common transformer configurations are shown in Figure 2.16. Figure 2.16 (a) shows a tapped structure consisting of an inner winding and an outer winding. Mutual coupling between adjacent conductors contributes mainly to the self-inductance of each winding. The structure is not often useful as the mutual inductance is small due to very little coupling. Figure 2.16 (b) shows two spirals interwound in the same plane. The interwound spirals ensures electrical characteristics of primary and secondary are identical, having the same number of turns. The transformer terminals are located in opposite sides allowing easy ac-



**Figure 2.16** Transformer Physical Structures (a) Tapped (b) Interleaved (c) Stacked

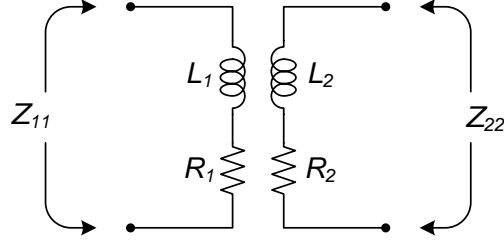
cess for layout. Figure 2.16 (c) shows two spirals stacked in separate metal planes. The advantage of the structure is a reduced overall area since it is implemented in different metal layers. The flux linkage between the two windings improve due to the close coupling. The coupling coefficient,  $k$ , can be as high as 0.9 for a stacked structure [19]. However, the use of separate metal planes results in an asymmetry between the primary and secondary windings caused by the different thickness and metal characteristics of the planes. This layout is suitable for low frequency operation as large capacitance between windings due to the overlap results in a low SRF. The advantages and disadvantages of each structures are summarized in Table 2.1.

**Table 2.1** Transformer Configuration Comparison

Configuration	Advantage	Disadvantage
Tapped	High SRF,	Large area and reduced $k$ coupling
Interleaved	Symmetrical. Moderate coupling	reduced SRF
Stacked	Area, high coupling	poor SRF

### 2.5.1 Transformer Model

A lossy transformer can be modeled with an inductor and a resistor in series for each winding representing the dominating series losses as shown in Figure 2.17. From the model, the characteristics of the transformer can be described. The impedance



**Figure 2.17** A Lossy Transformer Model

of the primary and secondary windings are,

$$Z_{11} = R_1 + j\omega L_1 \quad (2.9)$$

$$Z_{22} = R_2 + j\omega L_2 \quad (2.10)$$

The inductance of the primary and secondary windings are,

$$L_1 = \frac{\text{Im}(Z_{11})}{j\omega} \quad (2.11)$$

$$L_2 = \frac{\text{Im}(Z_{22})}{j\omega} \quad (2.12)$$

The quality factors of the windings are,

$$Q_1 = \frac{\text{Im}(Z_{22})}{\text{Re}(Z_{22})} \quad (2.13)$$

$$Q_2 = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} \quad (2.14)$$

To account for the imperfect coupling due to metal ohmic loss, substrate dissipation, parasitic capacitance and leakage [25], several parameters are defined. The k-factor represents the strength of the magnetic coupling and M is the mutual inductance between the primary and secondary windings as defined in Equation 2.15. For a perfectly coupled transformer, the k-factor is unity. But in a typical process, k is

between 0.6 and 0.9 for monolithic transformers [25]. The relation between coupling coefficient,  $k$ , and mutual inductance,  $M$ , is described in Equation 2.16.

$$M = \frac{Z_{12}}{j\omega} = \frac{Z_{21}}{j\omega} \quad (2.15)$$

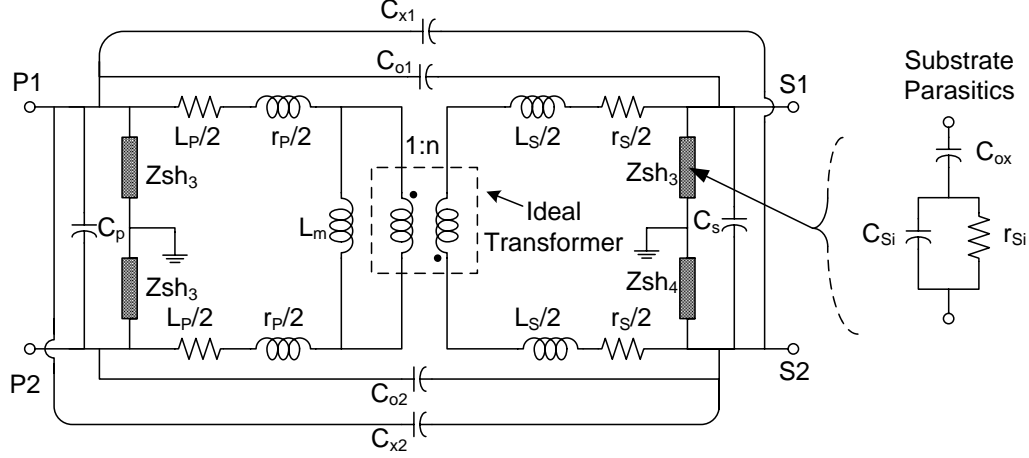
$$k = \frac{M}{\sqrt{L_1 \cdot L_2}} \quad (2.16)$$

### 2.5.2 Advanced Transformer Model

For accurate simulations, the simple lossy model in Figure 2.17 is not adequate to predict the behavior of monolithic transformer. A more advance transformer model is required to account for parasitics and losses specific to the process technology. One such model is from J. Long [19] and is shown in Figure 2.18. The lumped-element circuit model is based on extraction from the physical layout and process technology specifications using the GEMCAP2 computer program.

The core of the model is an ideal linear transformer with mutual inductance  $L_m$  and turn ratio of  $1:n$ , where  $n = L_s/L_p$ . Inductances  $L_p$  and  $L_s$  are placed in series with the primary and secondary windings of the linear transformer to account for the imperfect coupling or leakage of the magnetic flux between the windings. Resistors  $r_p$  and  $r_s$  are in series with the leakage inductances represent the ohmic losses in the windings. The losses are significant due to the relatively thin layers of metal available in the IC process. Interwinding capacitance is modeled by the capacitors connected between primary and secondary,  $C_o$  and  $C_x$ . Parasitic capacitances and dissipation in the substrate are represented by the shunt elements  $C_{ox}$ ,  $C_{si}$ , and  $r_{si}$ . Resistor  $r_{si}$  represents the losses caused by dissipation of the electric field in the substrate [19]. The current distribution across each conducting strip is frequency dependent due to proximity and skin effects, and introduces additional losses that increase proportionally to the square root of frequency. Hence,  $r_s$  is only valid for a narrow range of frequency. The substrate losses are represented by resistor  $r_{si}$  in

parallel with  $C_{si}$  as shown. The parasitic capacitances and resistance can be calculated from the equations found in [26].



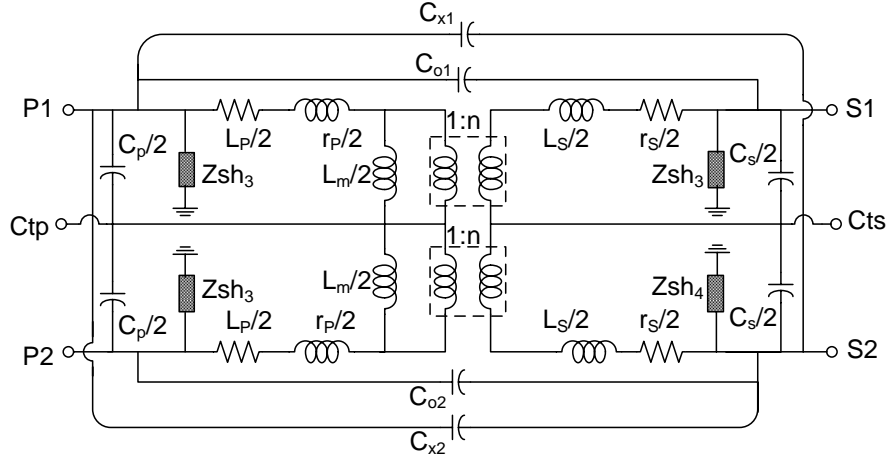
**Figure 2.18** 1:n Transformer Compact Model

### 2.5.3 Transformer Optimization

An optimal transformer structure requires attaining the desired bandwidth with the lowest possible loss while consuming as little chip area as possible. The same technique for optimizing inductor also applies to the transformer. Circular structure provides the lowest loss, design rule permitting. The interwinding capacitance introduced by closely spaced conductors is acceptable in most applications. Thicker metal reduces the ohmic losses in the primary and secondary windings of a planar transformer. Minimal spacing should be used between spirals for better magnetic coupling between primary and secondary windings. The self-inductance and associated parasitics at the secondary ( $L_s$  and  $C_{sox}$ ) are determined by the length and the winding and increase with increasing winding length.

### 2.5.4 A Transformer Design

In this work, a transformer was required to have an inductance of 1 nH at the primary and 390 pH at the secondary winding. The transformer is to be center-tapped, so symmetrical layout is important. SRF must be high enough as it needs to operate up to 10.6 GHz. To support center-tapping, a six port transformer model corresponding to the design is used, as seen in Figure 2.19. A center-tapped 2:1 square planar

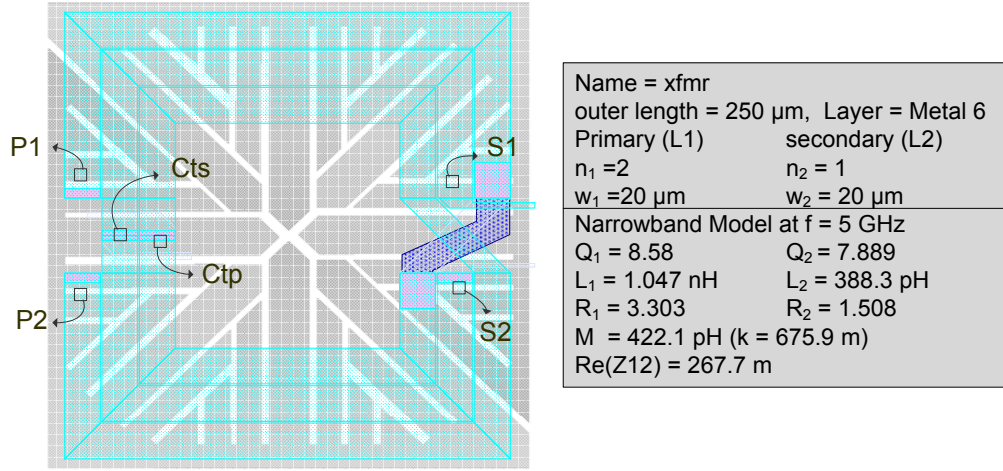


**Figure 2.19** 1:n Center-Tapped Transformer Compact Model

transformer with a dimension of  $250\ \mu\text{m}$  by  $250\ \mu\text{m}$  is designed to conform to design requirements as shown in Figure 2.20. The square symmetrical shape assures equal inductance of both sides of the center-tapped. The planar shape reduces capacitance improving SRF. The SRF of the primary inductor is located at 16.25 GHz while the secondary inductor is located at 41.61 GHz. The planar transformer has a coupling coefficient,  $k$ , of 0.6759 and a mutual inductance of 422.1 pH. The widths for both windings are  $20\ \mu\text{m}$  having a total of 3 turns. Minimal spacing of  $1\ \mu\text{m}$  allowable in the process was used to increase self and mutual inductance. The transformer was implemented on the metal-6 top layer for reduced metal resistivity and used in conjunction with a PGS to optimal Q. The transformer has a Q of 8.58 for the primary and 7.889 for the secondary windings. The transformer parameters were extracted



with the assistance of ASITIC at 5.2 GHz [27].



**Figure 2.20** 2:1 Square Planar Transformer

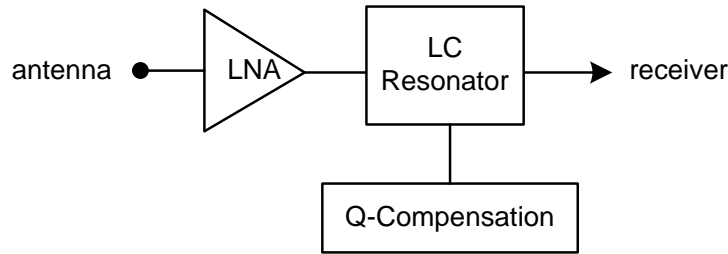
## 2.6 Summary

Integrated passive devices are essential for the realization of low cost integrated RF circuits. In this chapter, all the passive devices that are used in RFIC circuits were presented. Polysilicon resistor is popular due to the high resistance per area for polysilicon. Integrated capacitor uses large amount of silicon, the use of MIM capacitor saves valuable area. Design techniques were discussed to minimize the effect of process variations and mismatch. Accumulation mode MOS varactor offers linear capacitance tuning curve for better predictability while obtaining high  $Q$  and tuning ratio. Inductor and transformer remains the bottle neck for high  $Q$  RF circuits, particularly for integrated filters. The design and optimization of inductor and transformer remains a challenging area in RFIC designs. But thanks in part to accurate models over the last years and improved design tools, monolithic realization of inductor and transformer are becoming mainstream. However, advance 3D simulations of transformer are still needed for better accuracy for commercialization.

### 3. Active Q-enhanced LC Filter

The need for a high-performance, low-cost and single-chip RF receiver requires LC filters to be integrated. However, integrated LC filters have a low Q characteristic associated to the lossless monolithic inductor in a process, making it only useful in the receiver back-end where high Q requirement is not required. For RF front-end filtering, Q of at least 100 is required for channel-selection or band rejection in the gigahertz frequency. A requirement that is currently satisfied only by off-chip SAW filtering, but brings added cost and complexity to the receiver.

Using negative resistance compensation technique, the losses associated with LC filters can be compensated allowing the realization of a high Q RF front-end monolithic filter. Active Q-enhanced integrated filter uses an LC resonator with a Q compensation component to cancel the losses and an LNA to provide active gain as shown in Figure 3.1. At the RF front-end, input impedance matching is critical to

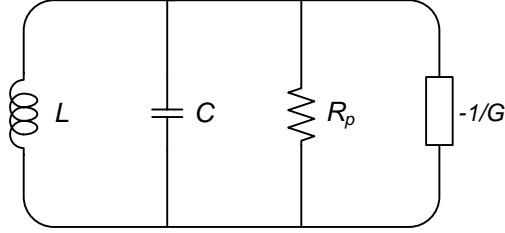


**Figure 3.1** An Active Q-enhanced LC Filter

the performance of the filter. In this chapter, active Q-enhanced filter theories are discussed followed by a discussion of input matching techniques for narrowband and ultrawideband applications.

### 3.1 LC Resonator Compensation

LC resonator filter relies on some form of loss compensation to increase the quality factor caused by the lossy on-chip passive devices. A primary method for increasing the Q is through the use of active devices to create a negative resistance [28] as shown in Figure 3.2.  $R_p$  represents the equivalent losses and  $-G$  represents the negative conductance for compensation. The total equivalent resistance of the resonator is given as  $R_{eq}$  as seen in Equation 3.1.



**Figure 3.2** LC Resonator with Q Compensation

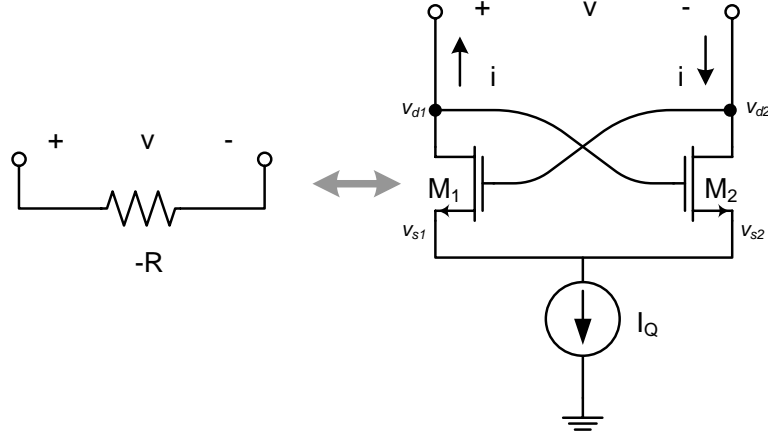
$$R_{eq} = R_p \parallel -1/G = \frac{R_p}{1 - R_p G} \quad (3.1)$$

By making  $-G$  equal to  $1/R_p$ , the resonator loss will be completely canceled resulting in an infinite Q as shown in Equation 3.2. However, if  $-G > 1/R_p$ , the resonator will oscillate.

$$Q = \frac{\omega_o}{BW} = \frac{R_{eq}C}{\sqrt{LC}} = R_{eq}\sqrt{\frac{C}{L}} \quad (3.2)$$

The cross-coupled MOSFET pair shown in Figure 3.3 is commonly used to generate the negative transconductance. The impedance as seen between the two terminals is given as  $R = -2/g_m$  by using the simple analysis given in Equation 3.3. However, at high frequencies, device parasitics and input resistance should be considered.

$$R = \frac{v}{i} = \frac{v_{ds1} - v_{ds2}}{i} = \frac{2v_{ds}}{-g_m \cdot v_{ds}} = \frac{-2}{g_m} = \frac{1}{-G} \quad (3.3)$$



**Figure 3.3** Cross-Coupled MOSFET Negative Transconductance

The transconductance,  $g_m$ , can be adjusted by varying the bias current,  $I_Q$  enabling for Q of the filter to be tunable. However, care must be taken as the resonator will oscillate if the negative resistance is greater than the losses in the resonator. Substituting for  $G = g_m/2$  in Equation 3.4 gives the following equivalent impedance equation for the resonator with Q-compensation.

$$R_{eq} = \frac{R_p}{1 - R_p G} = \frac{R_p}{1 - R_p (g_m/2)} = \frac{2R_p}{2 - R_p g_m} \quad (3.4)$$

### 3.1.1 Transformer Q-Enhancement

The Q-enhancement technique can also be used in a transformer to improve the quality factor of one winding to another. The advantage of transformer over inductor has been described in the previous chapter due to its mutual inductance. Transformers also have many uses, particularly in LNA and VCO (voltage controlled oscillator) to provide further Q improvement via coupling [24, 29]. The Q of the primary winding of a transformer, shown in Equation 3.5, can be enhanced by a negative generated

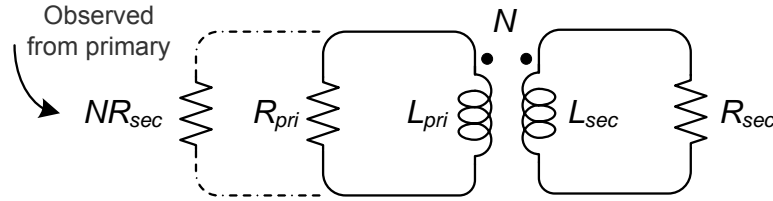
impedance circuit in the secondary winding.

$$Q_{pri} = R_{pri}\omega L_{pri} \quad (3.5)$$

A simple transformer model with equivalent parallel resistance and perfect coupling used to illustrate the concept is shown in Figure 3.4 where  $N$  is the inductance ratio between the primary and secondary windings, defined as  $N = L_p/L_s$ . Assume that the secondary inductor contains a cross-coupled negative transconductance circuit, shown in Figure 3.3, the equivalent secondary resistance,  $R_{sec}$ , is equal to,

$$R_{sec} = \frac{2R_p}{2 - R_p g_m} \quad (3.6)$$

When observing the impedance from the primary winding, the secondary impedance



**Figure 3.4** Transformer Impedance Transformation

is seen as  $R_{sec} \cdot N$  as shown in Equation 3.7.

$$\frac{V_p}{I_p} = \frac{V_s \sqrt{N}}{I_s / \sqrt{N}} = \frac{V_s}{I_s} \cdot N = R_{sec} \cdot N \quad (3.7)$$

Hence, the total impedance seen in the primary winding is equal to,

$$R_{pri} = R_p / (R_{sec} N) = \frac{R_{pri} R_{sec} N}{R_{pri} + R_{sec} N} \quad (3.8)$$

Substituting Equation 3.6 into Equation 3.8, the equivalent total resistance becomes,

$$R_{pri} = \frac{R_{pri}R_pN}{R_{pri} - (g_m/2)R_{pri}R_p + R_pN} \quad (3.9)$$

The Q of the primary winding then becomes,

$$Q_{pri} = \left[ \frac{R_{pri}R_pN}{R_{pri} - (g_m/2)R_{pri}R_p + R_pN} \right] \omega L_{pri} \quad (3.10)$$

The Q of the primary can be enhanced by increasing  $g_m$ . Maximum Q is obtained when  $g_m$  equals to,

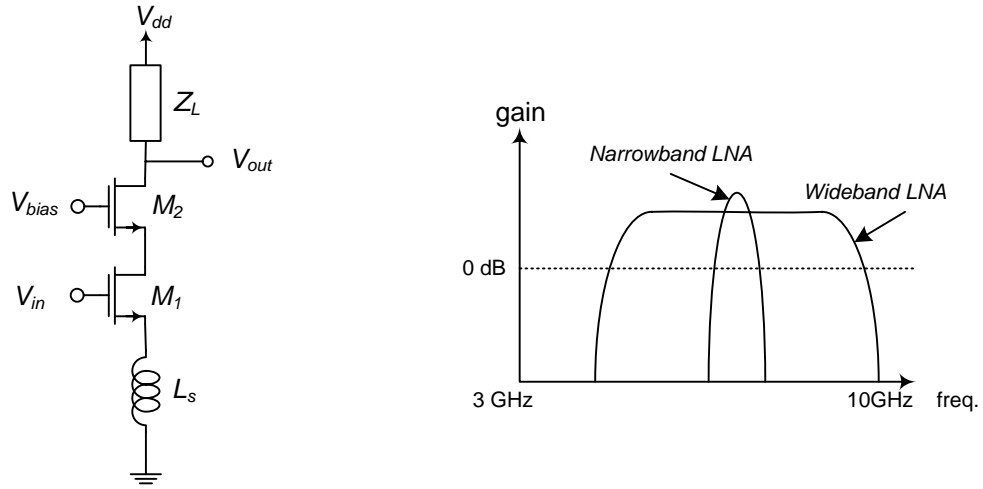
$$g_m = 2 \cdot \frac{R_{pri} + R_pN}{R_{pri}R_p} \quad (3.11)$$

## 3.2 Active Gain

The aim of the active gain stage in the filter is to amplify the signal such that it is suitable for subsequent stages. The active gain component compensates for the insertion loss in the filter which reduces the overall noise of the receiver as shown in Equation 1.2.

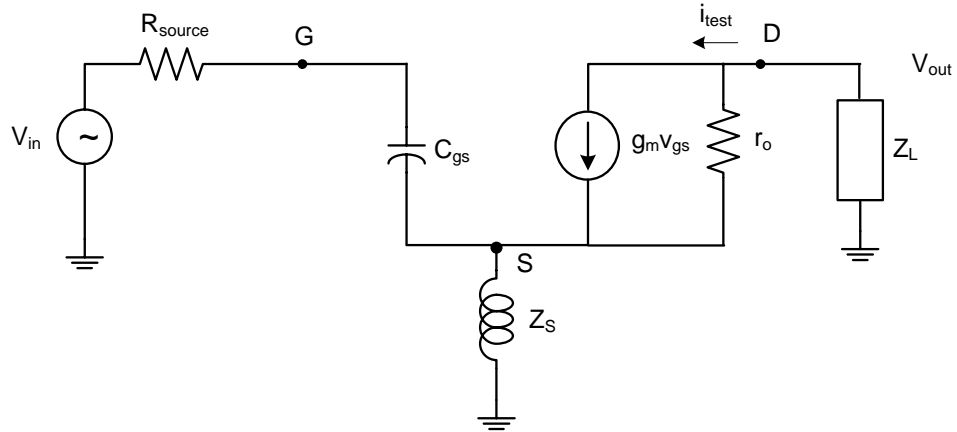
A cascode low noise amplifier (LNA) topology is an excellent choice for use as the active gain stage in an RF filter [30]. The cascode LNA configuration, shown in Figure 3.5, offers the benefits of increased input-output port isolation, good NF, high stability and gain. Part of the cascode LNA can be used as part of the input matching network reducing component counts as will be discussed later.

The impedance load,  $Z_L$ , determines whether the LNA is designed for an NB or UWB system. For NB,  $Z_L$  consists of either a high Q inductor or LC resonator for channel selection. For UWB, the bandwidth requirement is larger so the Q should be lower. Flat gain can be achieved throughout a wider bandwidth by using a combination of series resistor and inductor. The resistor provides improved gain at the lower frequency and the inductor at the upper frequency.



**Figure 3.5** Cascode LNA Configuration for NB or UWB

The transfer function (voltage gain) of the cascode LNA can be found by using the small signal model shown in Figure 3.6. To simplify the deviations, the body effect was ignored in the model. The cascode transistor,  $M_2$  is assumed to have a current gain of 1 and phase of zero and can be omitted in the model. The total impedance



**Figure 3.6** Simple Cascode LNA Small Signal Model

seen at the load,  $R_{totalout}$  is equal to the output impedance looking into D,  $R_{out}$ , in parallel with  $Z_L$ .

The voltage gain of the cascode LNA can be derived by placing a test current  $i_{test}$  at the drain, D. Hence,

$$V_{out} = i_{test} \cdot R_{out} \parallel Z_L \quad (3.12)$$

$$V_{out} = g_m v_{gs} \cdot R_{totalout} \quad (3.13)$$

To calculate the gain, one must first find the  $R_{out}$  and relate  $v_{gs}$  to  $v_{in}$ .

To find output resistance, add current test at output and ground input:

$$i_{test} = g_m v_{gs} + \frac{v_{ro}}{r_o} \quad (3.14)$$

$$v_{ro} = (i_{test} - v_{gs} g_m) r_o \quad (3.15)$$

$$i_{test} = \frac{v_s}{Z_S} \quad (3.16)$$

$$i_{test} = \frac{-v_{gs}}{Z_S} \quad (3.17)$$

$$v_{gs} = -i_{test} \cdot Z_S \quad (3.18)$$

Substitute  $v_{gs}$ .

$$v_{ro} = (i_{test} + i_{test} Z_S g_m) r_o \quad (3.19)$$

$$v_{ro} = (1 + Z_S g_m) \cdot r_o \cdot i_{test} \quad (3.20)$$

since

$$v_{test} = v_{ro} + v_s \quad (3.21)$$

$$v_{test} = v_{ro} - v_{gs} \quad (3.22)$$



Hence,

$$v_{test} = (1 + Z_S g_m) \cdot r_o \cdot i_{test} + i_{test} Z_S \quad (3.23)$$

$$\frac{v_{test}}{i_{test}} = (1 + Z_S g_m) r_o + Z_S \quad (3.24)$$

$$R_{out} = Z_S + r_o + Z_S r_o g_m \quad (3.25)$$

To get voltage gain, add a voltage  $v_{in}$ . Hence,

$$v_{gs} = v_{in} - i_{out} Z_S \quad (3.26)$$

$$i_{out} = g_m v_{gs} \quad (3.27)$$

$$i_{out} = g_m (v_{in} - i_{out} Z_S) \quad (3.28)$$

$$= g_m v_{in} - g_m i_{out} Z_S \quad (3.29)$$

$$i_{out} = \frac{g_m v_{in}}{1 + g_m Z_S} \quad (3.30)$$

Substitute:

$$v_{gs} = v_{in} - (g_m v_{gs}) Z_S \quad (3.31)$$

$$v_{in} = v_{gs} (1 + g_m Z_S) \quad (3.32)$$

$$v_{gs} = \frac{v_{in}}{1 + g_m Z_S} \quad (3.33)$$

Substitute:

$$v_{out} = -g_m v_{gs} R_{out} \parallel R_L \quad (3.34)$$

$$v_{out} = -g_m \cdot \frac{v_{in}}{1 + g_m Z_S} R_{out} \parallel R_L \quad (3.35)$$

$$v_{out} = -g_m \cdot \frac{v_{in}}{1 + g_m Z_S} Z_S + r_o + Z_S r_o g_m \parallel R_L \quad (3.36)$$

$$A_v = \frac{-g_m}{1 + g_m Z_S} \cdot \frac{Z_s R_L + r_o R_L + Z_s r_o g_m R_L}{Z_s + r_o + Z_s R_o g_m + R_L} \quad (3.37)$$

$r_o$  is the output resistance of the MOSFET and in saturation mode,  $r_o$  is very large. Therefore the above equation can be simplified by dividing the top and bottom equation by  $r_o$  and assuming  $r_o$  is infinity.

$$A_v \approx \frac{-g_m R_L}{1 + g_m Z_S} \quad (3.38)$$

$$A_v \approx -\frac{R_L}{Z_s} \quad (3.39)$$

Equation 3.39 shows that the gain of the LNA is mainly determined by the load impedance,  $R_L$  and the source impedance,  $Z_s$ .

### 3.3 Input Impedance Matching

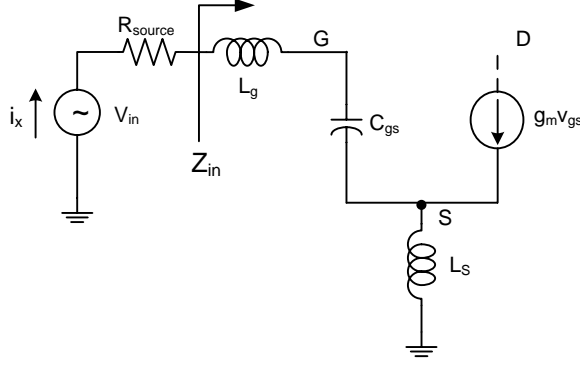
High performance RF receivers require input impedance matching to 50  $\Omega$  antenna. Matching minimizes insertion loss and reduces NF. Depending on whether the application is intended to operate over a narrowband or wideband spectrum, different matching networks are required.

#### 3.3.1 Narrowband Matching

The technique of simultaneous matching for power and noise for a narrowband LNA involves the use of an inductor,  $L_g$ , at the gate and  $L_s$  at the source of the input MOSFET. The small signal model of Figure 3.5 is shown below with an addition of  $L_g$ . The input of the LNA is matched to  $R_{source}$  which is equal to 50  $\Omega$ .

The analysis can be seen by first applying a test current,  $i_x$ , to find the input voltage ( $v_{in}$ ).

$$V_{in} = i_x \left( j\omega L_g - \frac{j}{\omega C_{gs}} \right) + i_x \left( 1 + \frac{g_m}{j\omega C_{gs}} \right) j\omega L_s \quad (3.40)$$



**Figure 3.7** Input Matching for NB LNA

Therefore, the input impedance,  $Z_{in}$  is equal to,

$$Z_{in} = \frac{V_{in}}{i_x} = j\omega L_g - \frac{j}{\omega C_{gs}} + j\omega L_s + \frac{g_m L_s}{C_{gs}} \quad (3.41)$$

To be matched, the real part of the input impedance must be equal to the source resistance  $R_{source}$ .

$$\frac{g_m L_s}{C_{gs}} = R_{source} \quad (3.42)$$

Therefore,

$$L_s = \frac{R_{source} C_{gs}}{g_m} \quad (3.43)$$

Equation 3.43 shows that by properly selecting the choice of  $L_s$ , a real impedance of  $50 \Omega$  can be seen at the input.

To match only to the real impedance, the imaginary part of the input impedance must equal zero. Therefore,

$$\omega L_g - \frac{1}{\omega C_{gs}} + \omega L_s = 0 \quad (3.44)$$

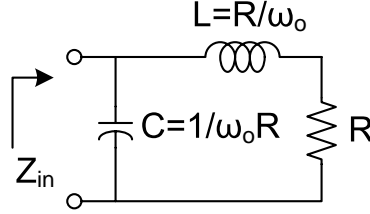
$$L_g = \frac{1}{\omega^2 C_{gs} - L_s} \quad (3.45)$$

Equation 3.45 shows that with proper choice of  $L_g$  and  $L_s$ , the parasitic capacitance

at the input can be eliminated leaving only the real impedance.

### 3.3.2 Wideband Matching

The NB technique demonstrated above is highly dependent on the frequency of operation, hence cannot be used for matching over a wideband of frequencies. Wideband matching presents a challenge, particularly over a 7.5 GHz bandwidth for the case of UWB. A technique known as wideband LC-Ladder Matching technique has been demonstrated in [31] that achieves better than -10dB of insertion loss from 3.1 GHz to 10.6 GHz. The technique involves using a second-order low-pass ladder filter shown in Figure 3.8.



**Figure 3.8** Second-Order Low-Pass Ladder Filter Section.

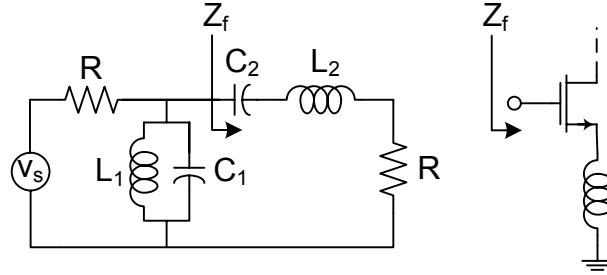
By choosing the values of  $L$  and  $C$  so that

$$L = \frac{R}{\omega_o} \quad (3.46)$$

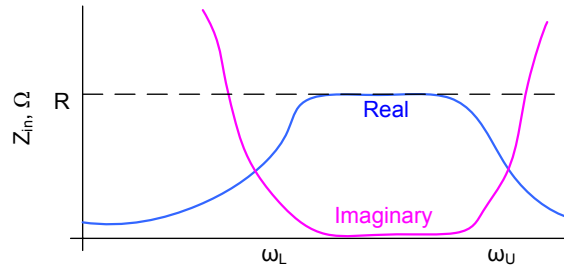
$$C = \frac{1}{\omega_o R} \quad (3.47)$$

The input impedance is mainly resistive and equal to  $R$ , given in Equation 3.42, to up to  $\omega_o$ , the low-pass filter cut-off frequency. Using the lowpass to bandpass transformation  $((s/\omega_o) \rightarrow (s/\omega_o) + (\omega_o/s))$ , the series inductor is transformed to a series LC and the shunt capacitor to a parallel LC [31]. In Figure 3.9, the right side of the bandpass ladder filter circuit is similar to the input impedance of an inductively

generated LNA. Hence, the input impedance of an LNA can be used as part of the a wideband impedance matching network circuit.



**Figure 3.9** Fourth-order Bandpass Ladder Filter Used for Impedance Matching



**Figure 3.10** Input impedance of the Bandpass Filter Versus Frequency

Figure 3.10 shows the input impedance of the fourth-order bandpass ladder filter. The input impedance is matched to  $R$  from the lower frequency,  $\omega_L$ , to the upper frequency  $\omega_U$ . The approximated equations for choosing the matching inductors and capacitors are shown in Equations 3.48 and 3.49.

$$L_1 \approx \frac{R}{\omega_L} \quad \text{and} \quad C_2 \approx \frac{1}{\omega_L R} \quad (3.48)$$

$$L_2 \approx \frac{R}{\omega_U} \quad \text{and} \quad C_1 \approx \frac{1}{\omega_U R} \quad (3.49)$$

### 3.4 Q-enhanced Filter Summary

Active Q-enhanced filters make the everlasting goal of a complete monolithic transceiver achievable as it solves the limitation of low Q in integrated filter. The filter can be utilized in many receiver architectures to improve performance and reduce receiver component count and complexity. In a heterodyne receiver, filters are used to provide improved image rejection and channel-selection which eliminates the need of off-chip filters, allowing the receiver to be fully integrated. In a homodyne receiver, the preselection filter and LNA can be replaced with an active Q-enhanced filter at the RF front-end. This will relax the performance requirement of preceding filters.

Q-enhanced filter relies on negative generation technique to compensate for the loss in the LC filter. The technique can be used directly in parallel with the inductor or in the secondary winding coupled to the primary winding of a transformer. The degree of compensation can be varied by adjusting  $g_m$  which allows for the gain and bandwidth of the filter to be tunable. However, care must be taken to ensure that the negative compensating resistance is not larger than the loss as this will lead to the filter becoming an oscillator.

Input impedance matching is important to the overall performance of the filter. A matched input impedance reduces insertion loss and minimizes NF. Simultaneous matching for power and noise is only valid over a small narrowband frequency. For wider bandwidth matching, the wideband LC-ladder matching technique can be used. In the next chapter, the conventional active Q-enhanced filter covered in this chapter will be modified to develop a dual mode Q-enhanced filter providing bandpass filtering in NB and gain to UWB while rejecting the NB interference at 5 GHz.

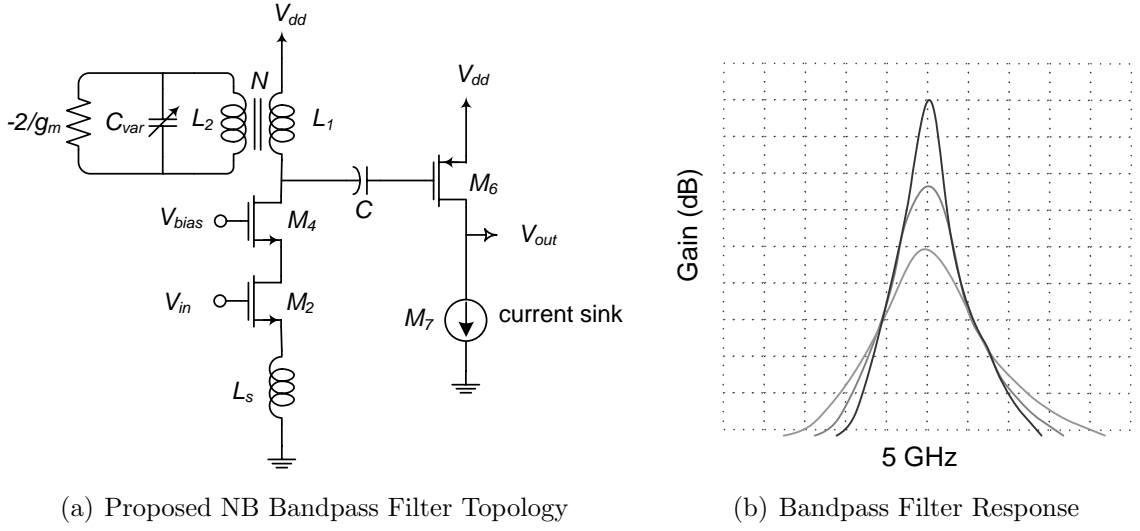
## 4. A Dual Mode Q-enhanced NB and UWB Filter with Interference Rejection

Low cost monolithic transceiver solution is the driving force behind today's research in RFIC designs. A bottle neck preventing fully integrated monolithic design is the low Q in integrated filter. In the previous chapter, the Q-enhanced active filter has shown to be the solution. The next area of RFIC research is to make the transceiver more functional by making it operable over multiple frequencies and standards. This allows RF applications to benefit by being compatible with multiple technologies.

In this chapter, a Q-enhancement front-end filter is proposed to take advantage of the co-existence between 802.11a and UWB providing dual mode functionality in a receiver. Low cost and low complexity are achieved by using a direct sampling receiver architecture with a Q-enhancement filter for channel selection at the RF front-end. A Q-enhancement technique using transformer coupling is proposed to provide the bandpass filtering in an NB system. The same technique is used for 802.11a interference rejection for UWB allowing the receiver to operate from 3.1 GHz up to 10.6 GHz.

### 4.1 A Q-enhanced Bandpass Filter

The bandpass filter for 802.11a requires a BW range of 5.15 to 5.35 GHz. The filter must be able to select and filter out a channel of 20 MHz within the 200 MHz bandwidth. Good input impedance matching at 5 GHz is required for low noise and optimal transfer. A proposed topology for the NB bandpass filter consists of a cascode



**Figure 4.1** Q-enhanced Bandpass Filter and Response in NB Mode

LNA with degeneration inductor for high linearity, and a Q-enhanced LC resonator load is shown in Figure 4.1. The LC resonator uses a cross-coupled pair to provide the negative resistance equivalent to  $-2/g_m$ . The resonator is coupled to the LNA via a transformer to provide a high impedance at 5 GHz resonance frequency. An accumulation mode varactor, shown in Figure 2.6, is used to provide frequency tuning from 5.15 GHz to 5.35 GHz. A second stage amplifier with an active load is used to drive a  $50 \Omega$  impedance port and to integrate with the UWB notch filter which will be discussed later.

The proposed NB bandpass filter has a resonance frequency located at,

$$f_o = \frac{1}{2\pi\sqrt{(L_2 + M)C_{var}}} \quad (4.1)$$

where

$$M = k\sqrt{L_2 \cdot L_1} \quad (4.2)$$

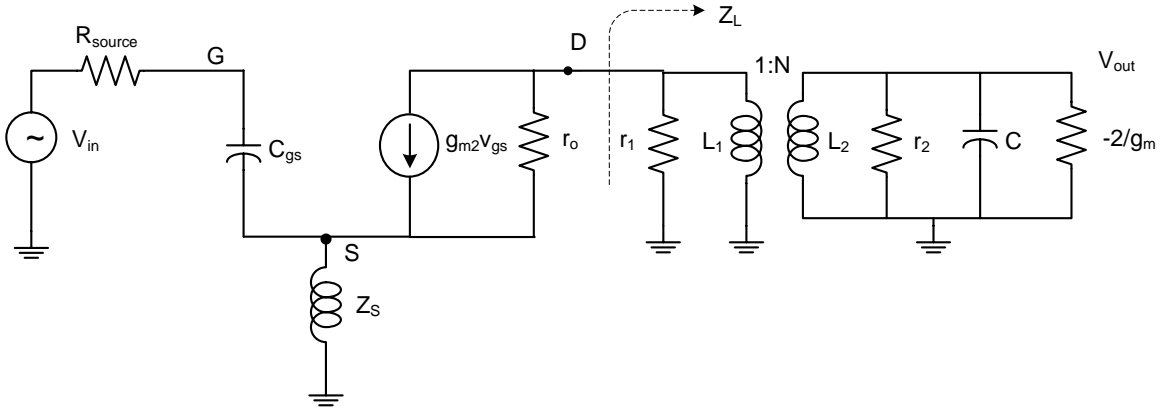


## Small Signal Analysis

The gain of the filter can be expressed as the gain of the first stage LNA multiplied by the gain of the second stage as shown in Equation 4.3.

$$A = \frac{v_{out}}{v_{in}} = A_{v1} \cdot A_{v2} \quad (4.3)$$

For the analysis of the first stage, the response of the filter can be expressed as the small signal equivalent circuit shown in Figure 4.2. To simplify the analysis, the transformer is assumed to be lossless where  $k=1$ .  $N$  represents the inductor ratio between the primary winding,  $L_1$ , and secondary winding,  $L_2$ . The parallel equivalent resistance of  $L_1$  is given as  $r_1$  and the parallel resistance of  $L_2$  and  $C$  is equal to  $r_2$ . The negative resistance has a value of  $-2/g_m$  for the cross-coupled pair. Let the



**Figure 4.2** Proposed Bandpass Small Signal Model for First Stage

impedance seen from the load equal to  $Z_L$ , the gain equation has the form similar to Equation 3.37. Replacing  $R_L$  with  $Z_L$ , the gain equation becomes,

$$A_{v1} = \frac{-g_m}{1 + g_m Z_S} \cdot \frac{Z_s Z_L + r_o Z_L + Z_s r_o g_m Z_L}{Z_s + r_o + Z_s R_o g_m + Z_L} \quad (4.4)$$

At resonance frequency, the high impedance from the secondary winding is trans-

formed to the primary winding increasing the load impedance of the LNA. To calculate  $Z_L$ , at the resonance frequency, the impedance of the secondary winding must first be transformed to the impedance seen in the primary. Assuming perfect coupling, the equivalent impedance of the secondary observed from the primary is  $N \cdot R_{eq}$ . From Equation 3.4, the equivalent total resistance in the secondary winding is equal to,

$$R_{eq} = \frac{2r_2}{2 - g_m} \quad (4.5)$$

The impedance seen in the primary winding is  $N \cdot R_{eq}$ .

Therefore,  $Z_L$  at resonance equals to

$$Z_L = \frac{r_1 \cdot NR_{eq}}{r_1 + NR_{eq}} \quad (4.6)$$

$$Z_L = \frac{r_1 N \left( \frac{2r_2}{2 - g_m} \right)}{r_1 + N \left( \frac{2r_2}{2 - g_m} \right)} \quad (4.7)$$

which simplifies to,

$$Z_L = \frac{2Nr_1r_2}{2r_1 + 2Nr_2 - g_mr_1} \quad (4.8)$$

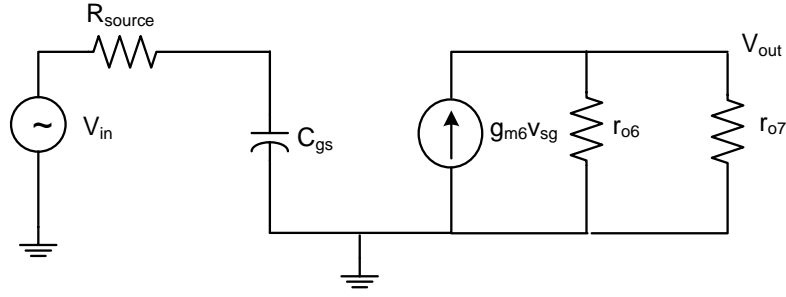
Hence, in theory, infinite Q can be obtained when

$$g_m = \frac{2(r_1 + r_2N)}{r_1} \quad (4.9)$$

If the output impedance,  $r_o$ , of the transistor is omitted and assumed  $g_{m2}$  is large, which is usually the case for LNA, then the filter response is shown to be dominated by the load impedance,  $Z_L$ , and the degeneration impedance,  $Z_s$ ,

$$A_{v1} \approx \frac{-g_{m2}Z_L}{1 + g_{m2}Z_s} \approx \frac{-Z_L}{1/g_{m2} + Z_s} \approx \frac{-Z_L}{Z_s} \quad (4.10)$$

Substituting for  $Z_L$  and  $Z_s$ , the gain of the first stage filter is approximately given



**Figure 4.3** Small Signal Model of the Second Stage Amplifier with Current Sink

as,

$$A_{v1} \approx \frac{1}{\omega L_s} \cdot \frac{2Nr_1r_2}{2r_1 + 2Nr_2 - g_m r_1} \quad (4.11)$$

The second gain stage is given by the small signal model shown in Figure 4.3. The resistance of the current sink, M7, is represented as  $r_{o7}$ .

By inspection, the gain is equal to Equation 4.13.

$$A_{v2} \approx g_{m6} \cdot \frac{r_{o6}r_{o7}}{r_{o6} + r_{o7}} \quad (4.12)$$

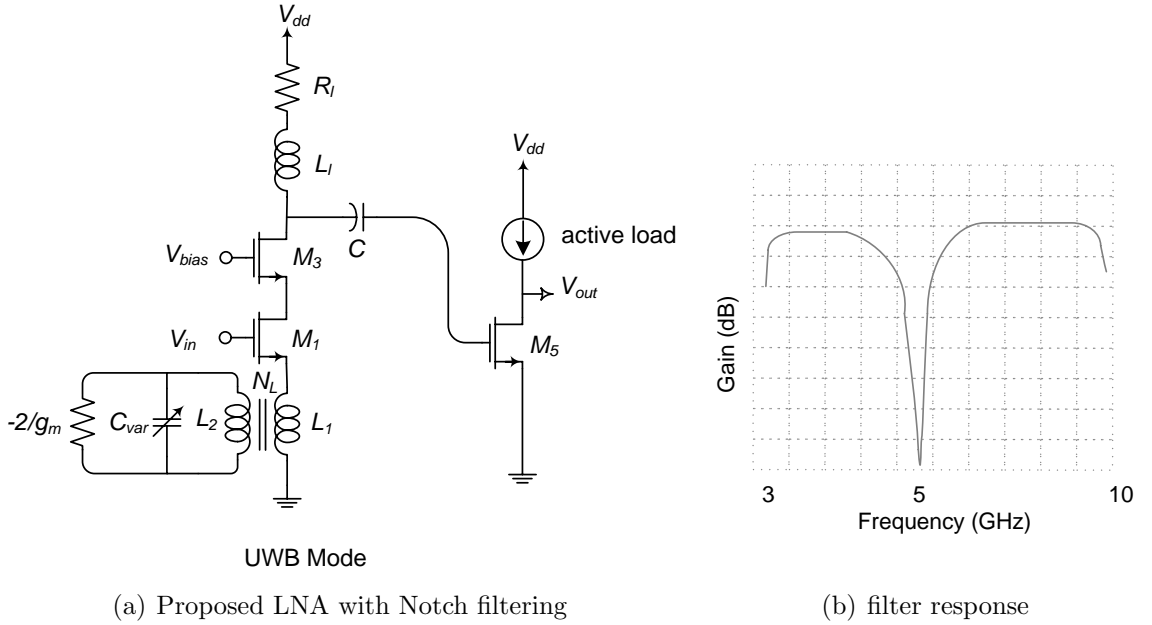
The total gain of the filter is equal to Equation 4.13.

$$A_{total} = A_{v1} \cdot A_{v2} \approx \frac{1}{\omega L_s} \cdot \frac{2Nr_1r_2}{2r_1 + 2Nr_2 - g_m r_1} \cdot g_{m6} \cdot \frac{r_{o6}r_{o7}}{r_{o6} + r_{o7}} \quad (4.13)$$

Equation 4.13 states that the gain of the bandpass filter is dominated by the value of  $g_m$  in the first stage. The transconductance,  $g_m$ , needs to be large in order to cancel the loss in the secondary,  $r_2$ , and primary,  $r_1$ , windings. A large inductance ratio,  $N$ , will improve the filter linearity but will require a larger Q current to increase  $g_m$ . It also reduces the SRF of the transformer. Hence, an N=2:1 transformer was used for the design which can be found in Figure 2.20.

## 4.2 A UWB LNA with NB Interference Rejection

A filter topology consisting of a wide band LNA along with a Q-enhanced notch filter is proposed for the UWB receiver is shown in Figure 4.4(a). The first stage consists of a wideband LNA with a Q-enhanced resonator coupled at the degeneration inductor,  $L_1$ . The resonator is centered at 5 GHz providing notch filtering to the NB interference. A second stage of the filter is an active load amplifier which provides additional amplification to the signal of interest and acts as a buffer to drive a  $50\ \Omega$  load. The response of the filter is shown in Figure 4.4(b).



**Figure 4.4** An UWB LNA with Notch Filter Topology and Response

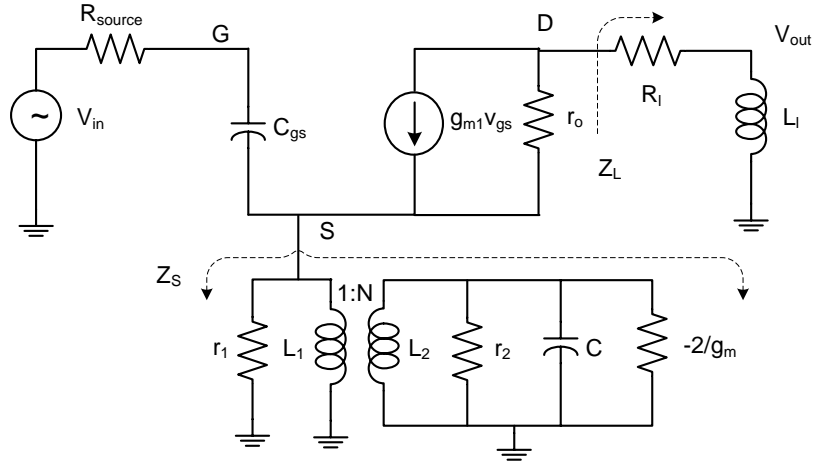
The inductor load,  $L_l$ , provides gain at high frequencies and the resistor load,  $R_l$  to low frequencies. This will achieve a gain flatness across the wide bandwidth [32]. Negative mutual coupling across the transformer windings  $L_1$ , and  $L_2$ , are used to reduce the effective inductance of the degeneration inductor. The frequency of

resonance is therefore given by the following equation.

$$f_o = \frac{1}{2\pi\sqrt{(L2 - M)C_{var}}} \quad (4.14)$$

### Analysis of First and Second Stage Gain

The gain response of the filter at the resonance frequency is analyzed below,



**Figure 4.5** Small Signal Model of First stage LNA with Notch Filtering

From inspection, the gain equation of the first stage has the form of,

$$A_{v1} \approx \frac{-g_{m1}Z_L}{1 + g_{m1}Z_S} \quad (4.15)$$

where  $Z_L = R_l + sL$  and from Equation 4.8,

$$Z_S = \frac{2Nr_1r_2}{2r_1 + 2Nr_2 - g_mr_1} \quad (4.16)$$

Hence,

$$A_{v1} \approx \frac{-g_{m1}(R_l + \omega L)}{1 + g_{m1}} \cdot \frac{2r_1 + 2Nr_2 - g_mr_1}{2Nr_1r_2} \quad (4.17)$$

For the second gain stage, the gain is simply given as,

$$A_{v2} = g_{m6}(r_{05}||r_{o6}) \quad (4.18)$$

The total gain is therefore equal to,

$$G = A_{v1} \cdot A_{v2} \approx \frac{-g_{m1}(R_l + \omega L)}{1 + g_{m1}} \cdot \frac{2r_1 + 2Nr_2 - g_{m1}r_1}{2Nr_1r_2} \cdot g_{m5}(r_{05}||r_{o6}) \quad (4.19)$$

At the resonance frequency, the filter has a notch response. Away from this frequency, the filter will act as an LNA. At frequencies below the resonance frequency,  $Z_S$  will appear inductive, approximately equaling to  $L_1 + M$ . At frequencies above the resonance frequency, the resonator appears capacitive which makes  $Z_S$  appear capacitive.

Equation 4.20 shows that a larger  $g_m$  value is required to cancel both  $r_2$  and  $r_1$  to increase the depth of the notch.

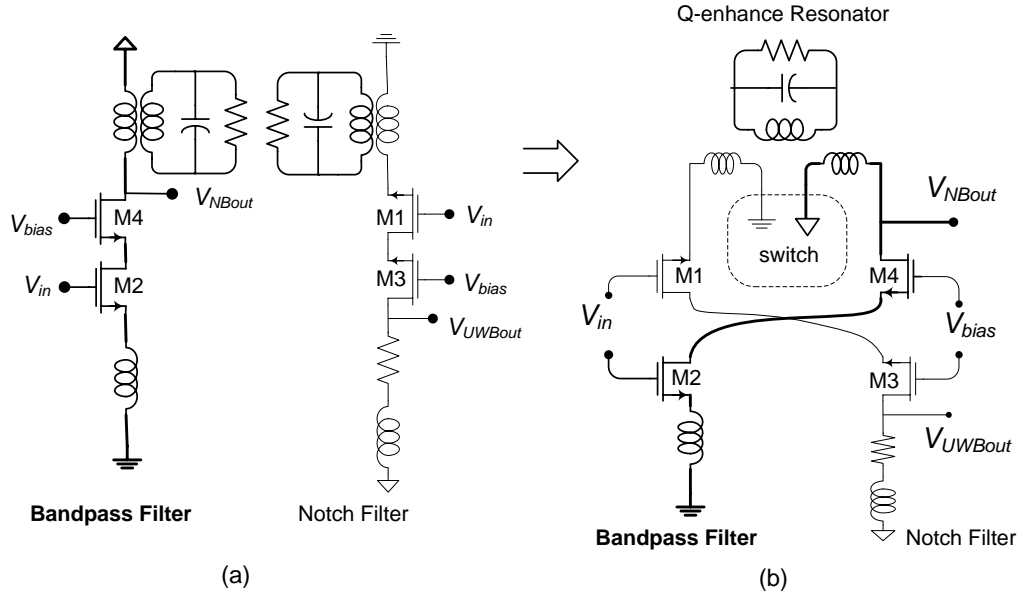
$$G \approx A_{v1} \cdot A_{v2} \approx \frac{-g_{m1}Z_L}{1 + g_{m1}(r_1||\omega L_1)} \cdot g_{m5}(r_{05}||r_{o6}) \quad (4.20)$$

This equation shows that the gain above and below the resonance frequency is obtained both from the first and second stage. Hence, above and below the resonance frequency, the filter acts as a wideband LNA.

### 4.3 A Dual Mode Q-Enhanced Filter

The proposed bandpass filter for 5 GHz WLAN and the UWB LNA with NB interference rejection filter topology is very similar in the first gain stage. The placement of the Q-enhancement circuit determines its bandpass or notch behavior. Conceptually, the two filters can be combined, as shown in Figure 4.6. To develop a dual mode filter that can provide both bandpass and notch filtering, the two basic filter topologies is connected together at the switch point. The switch is implemented to

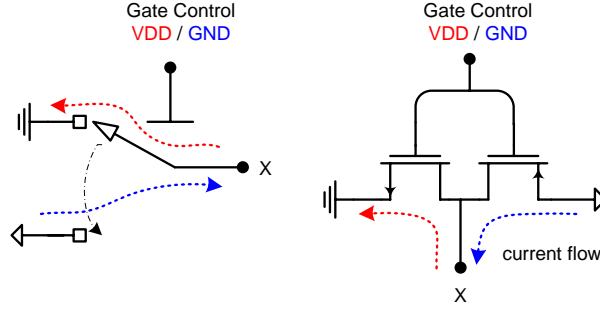
alternate between Vdd and GND, depending on a mode control signal turning on either notch or bandpass filtering. The combination results in the use of a single resonating circuit for both bandpass filter and notch filter modes. In the design, when the switch is connected to Vdd, the dual mode filter behaves as a 5 GHz NB bandpass channel-select filter. When the switch is connected to GND, a wideband LNA with a 5 GHz notch filter to eliminate the NBI in UWB is realized.



**Figure 4.6** (a) A Bandpass and an LNA With a Notch Filter Shown Upside Down (b) Dual Filter Integration

### 4.3.1 The Mode Switch

A switch to select the mode of operation for the filter was realized using an NMOS and PMOS transistor. The gates are connected to a digitally controlled signal that alternates between 1.8 V and 0 V as shown in Figure 4.7. Similarly to an inverter, when the gate is at 1.8 V, the NMOS pulls the current from 'x' to ground. When the gate is at 0 V, the current flows from VDD to point 'x'. Thus, the switch provides a voltage potential which controls the direction of current flow turning on either



**Figure 4.7** a) Concept Switch b) Realized MOSFET Switch

the bandpass or notch filter. Parasitic capacitances and resistances in the MOSFET switch will affect the switching speed and the RF performance of the filter. The high frequency behavior of the switch can be modeled with moderate accuracy [33] using the small-signal model shown in Figure 4.8. When the transistor is on, the drain to source resistance,  $r_o$ , is small as it is in the subthreshold region. The switch will have parasitic capacitance at each junction as modeled by the capacitances gate to source  $C_{gs}$ , gate to drain  $C_{gd}$ , source to bulk  $C_{sb}$  and drain to bulk  $C_{db}$ . The parasitic capacitances  $C_{sb}$  and  $C_{db}$  are small as the voltage potential between source, drain and bulk is very small, in which case, it can be ignored. In this simplified model, the  $C_{gs}$  and  $C_{gd}$  is approximately equal to,

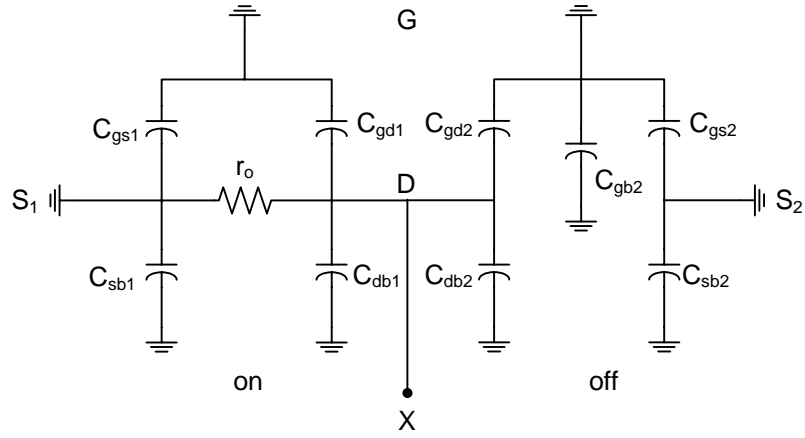
$$C_{gs} = C_{gd} = \frac{WLC_{ox}}{2} \quad (4.21)$$

When the transistor is off, the drain to source resistance,  $r_o$ , will be large which can be omitted from the model. Since the channel has disappeared,  $C_{gs}$  and  $C_{gd}$  are much smaller. The dominating capacitances are the overlap and the infringing capacitances [33].

$$C_{gs} = C_{gd} = WL_{ov}C_{ox} \quad (4.22)$$

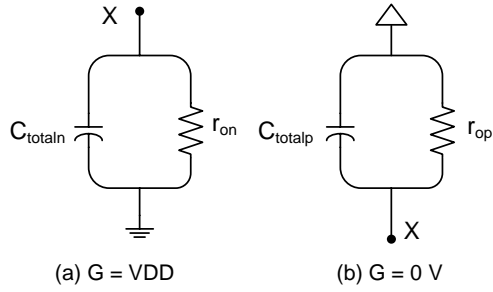
At any time, the switch will have one transistor on and one off. The gate (G), sources (S1 and S2) will act as an AC ground. The simplified model for the transistor,





**Figure 4.8** Small Signal Mode of the Complete Switch

derived, is shown in Figure 4.9 for a) NMOS turned on b) PMOS turned off. The



**Figure 4.9** a) X is Connected to Ground b) X is Connected to VDD

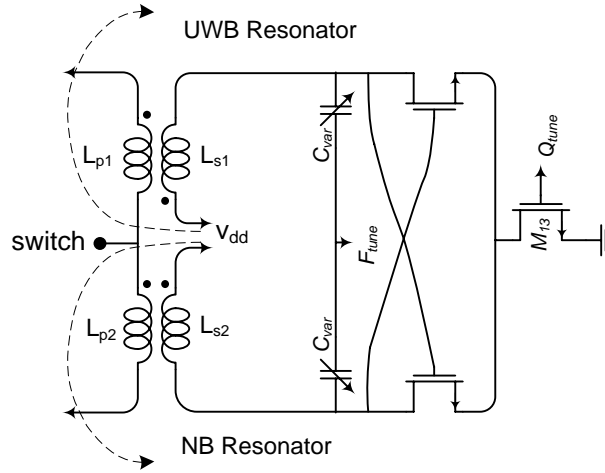
total equivalent capacitance for an NMOS and PMOS MOSFET in the switch are equal to,

$$C_{totaln} = C_{gdn} + C_{dbp} + C_{gdp} \quad (4.23)$$

$$C_{totalp} = C_{dbn} + C_{gdn} + C_{gdp} \quad (4.24)$$

The dominating capacitance is  $C_{gd}$  for both  $C_{totaln}$  and  $C_{totalp}$  since the capacitance of the transistor that is off is much smaller [33].

The switch resistance will contribute to the series resistance of the primary wind-

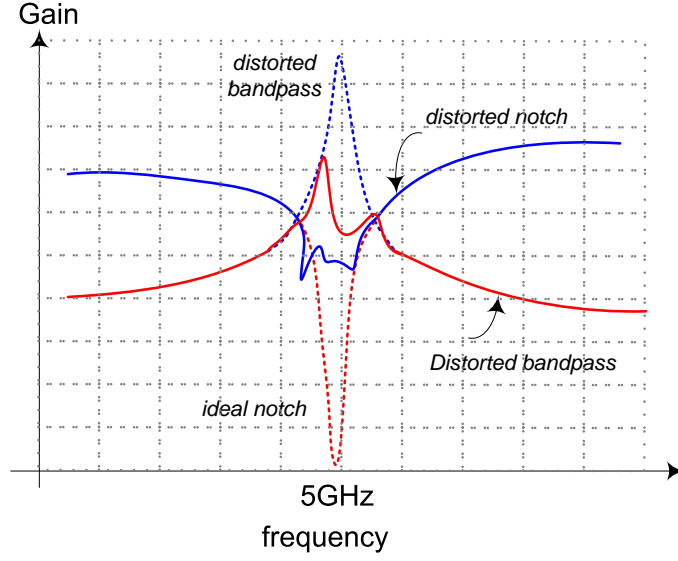


**Figure 4.10** Q-enhancement Resonator

ing of the transformer decreasing the  $Q$  of the filter. As a result, larger current is needed to generate the negative resistance required to cancel out the loss. Hence, the NMOS and PMOS transistors must be made large to decrease the resistance across the switch. The drawback of large transistor is an increase in parasitic capacitances. At a particular frequency, the capacitance will resonate with the inductance in the primary winding providing a low impedance to ground. However, since the resonance frequency is far away from the operating frequency range, this will not present a problem.

### 4.3.2 Q-enhance Resonator

A transformer-based Q-enhancement resonator circuit for the dual mode filter design is shown in Figure 4.10. The circuit consists of a center-tapped transformer with 2:1 primary to secondary windings. The center-tap of the primary winding is used for mode switching. Two accumulated mode MOS varactors are used to tune the resonant frequency. The  $Q$  of the filter is tunable by adjusting the current via the voltage,  $Q_{tune}$ . Essential, the circuit has two separate resonators with the same tuning points for frequency and  $Q$  tuning. The NB resonator consists of  $L_{s2}$ ,  $C_{var}$



**Figure 4.11** Resonator Distortion

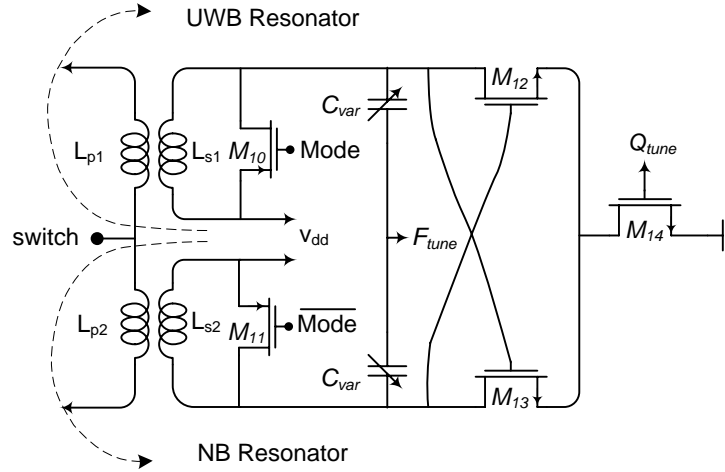
and a negative impedance,  $-1/g_m$ . The UWB resonator consists of  $L_{p1}$ ,  $C_{var}$  and a negative impedance,  $-1/g_m$ . Since the coupling of  $L_{p2}$  and  $L_{s2}$  is positive, the NB resonance frequency is equal to,

$$f_o = \frac{1}{2\pi\sqrt{(L+M)C}} \quad (4.25)$$

$L_{p1}$  and  $L_{s1}$  is negatively coupled which results in a UWB resonance frequency of,

$$f_o = \frac{1}{2\pi\sqrt{(L-M)C}} \quad (4.26)$$

Because the two resonators will resonate at the same frequency, there will be some distortion in the response as shown in Figure 4.11. This is because the NB and UWB resonators are interlinked at the switch. The affect can be further understood by analyzing the terms in the first stage of the NB and UWB filters in Equation 4.11 and 4.17. The same terms  $2r_1 + 2Nr_2 - g_mr_1$  appear in the nominator for NB and denominator for UWB. Since the UWB and NB filters are integrated at the switch, the



**Figure 4.12** Two Q-enhancement Resonators Utilizing the Same  $F_{tune}$  and  $Q_{tune}$  Point

same terms appear in both the nominator and denominator of the transfer function equation causing distortion in the response.

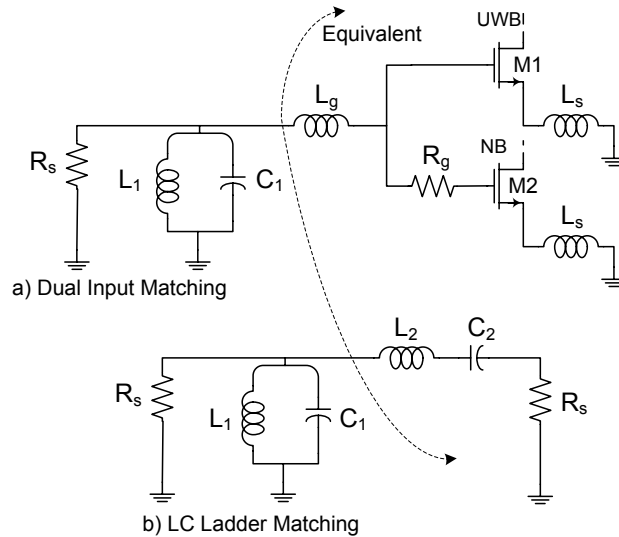
The distortion was resolved by adding a PMOS switch in parallel with each resonator, as shown in Figure 4.12, to ensure the resonators don't resonate at the same frequency. The same mode control signal can be applied to the gate to select the appropriate resonator. When 'mode' equals to 0 V, the PMOS switch is on. This results in a low resistance in parallel with the resonator which causes the quality factor to drop, hence disabling the Q-enhancement effect. When 'mode' is equal to 1.8 V, the PMOS switch is off. At this point, it is equivalent to a large resistor in parallel with the resonator which has minimal effect on the Q of the resonator. The PMOS transistor will turn on and odd the resonators isolating them during the NB and UWB mode switch.

The drawback of using the PMOS switch is that the overall capacitance of the resonator increases resulting in a smaller tuning range for the MOS varactor. It also decreases the overall Q of the resonator which requires more current to make  $g_m$  larger. One advantage is that the individual PMOS transistor can be sized to allow the two resonators to resonate with the same matching frequency tuning. That is, the

primary and secondary windings of the NB resonator has a positive coupling while the UWB resonator has a negative coupling resulting in a lower overall inductance. In the design, the transistors M10 and M11 have a width of  $632\ \mu m$  and  $592\ \mu m$ , respectively. The different sizing accounts for different capacitive parasitics enabling the two resonators to be tuned at the same frequency.

### 4.3.3 Input Matching

To simplify the design of the filter and reduce complexity when integrating to a receiver, the input gates of the NB and UWB LNA are connected together. This will enable the filter to selectively receive either NB or UWB signals at the same antenna [34]. This means that only one input impedance matching network is required. For matching both narrowband at 5 GHz and wideband from 3.1 GHz to 10.6 GHz simultaneously, a combination of the wideband LC-Ladder technique and conventional NB matching technique are used. The matching network and equivalent small signal model is shown in Figure 4.13.

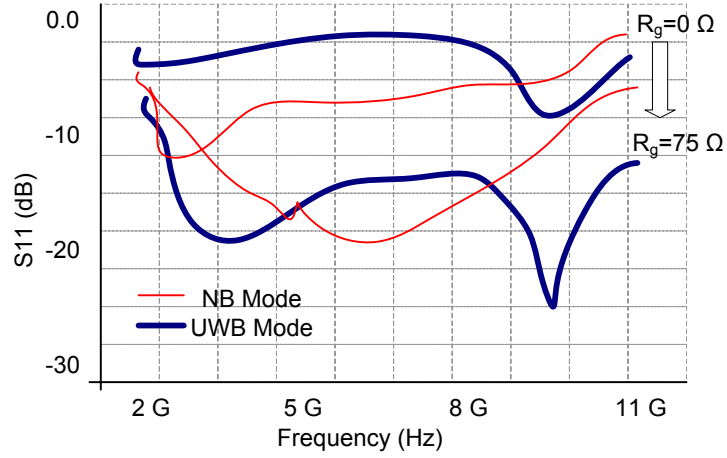


**Figure 4.13** a) Modified Wideband Ladder Matching for NB and UWB Dual Input  
b) LC Ladder Matching

In either NB or UWB mode, the MOSFETs, M1 and M2, will alternate between operating in the subthreshold and the saturation region due to the switching of the Mode Switch circuit. As the result, the  $g_m$  of the MOSFET varies from small to large. Since the two MOSFETs are in parallel, the overall real impedance of the input is too low to match to the  $50\ \Omega$ .

Several modifications to the wideband LC Ladder matching network are required to match the input impedance for both the NB and UWB filter. The inductances,  $L_s$ , must be large enough to cancel the gate to source parasitic capacitances in the MOSFETs. The consequence of this is that large degeneration inductor results in a low gain filter. To eliminate the requirement for large degeneration inductor,  $L_g$  is added at the gates of M1 and M2 to provide additional inductance allowing  $L_s$  to be kept small for high filter gain.

In the UWB mode, M2 is in the triode region resulting in a small  $g_m$ , therefore, it is difficult to match to  $50\ \Omega$  input impedance as given in Equation 3.42. Simulation was used to aid with determining the ideal size for  $R_g$  as shown in Figure 4.14. As the



**Figure 4.14** Determining Optimal  $R_g$  Value

value of  $R_g$  increases, the input impedance matching improves. Adding a resistor to the gate of M2 increases the NF in the NB mode. However, NF of the UWB decreases

due to more power being directed towards the gate of M1. The value of  $R_g$  was chosen to balance the NF between the two modes. Overall, the addition of  $L_g$  and  $R_g$  makes matching for both modes possible. Capacitor  $C_p$  is used for low frequency matching. To increase  $C_2$ ,  $C_p$  was added in parallel with  $C_{gs}$  of M2 to increase the capacitance. Simulation shows this technique achieves better than -10 dB input matching in UWB from 3.1 GHz to 10.6 GHz. It also achieves a good matching of better than -15 dB in NB mode at 5 GHz but at the cost of higher NF.

#### 4.3.4 Final Dual Filter Circuit

The complete dual mode filter schematic with bias circuitries is shown in Figure 4.15. The voltage at *Mode* is used to control the switch ( $M_8$  and  $M_9$ ) and the resonators via  $M_{10}$  and  $M_{11}$ . When the signal at *Mode* is LOW, the switch is connected to 1.8V and the dual filter behaves as a bandpass filter. When *Mode* is HIGH, the switch is grounded and the dual filter behaves as an UWB LNA with notch filtering capability. Both modes share the same input, output, Q tuning and frequency tuning. To prevent the signals in the resonator and LNA from coupling during filter layout, the resonator is connected to a separate power supply via  $V_{dd2}$ . A current source ( $M_7$ ) provides a current of 100  $\mu A$  to bias  $M_1$ ,  $M_2$  and  $M_5$ . The first stage LNA consumes 4-5 mA and the second stage consumes 2-3 mA of currents. About 3 to 5 mA of current is required to drive the Q-enhancement resonators depending on the Q tuning voltage.

#### Passive Device Parameters

The proposed filter attempts to reduce die area by utilizing only five inductors and one transformer in the design. The layout and optimization of all the resistors, capacitors, varactor, inductors and transformer can be found in Chapter 2: Integrated Passive Devices. Table 4.1 summarizes the values and dimensions.





**Table 4.1** Passive Device Parameters

Passive Device	Values	Dimension / radius ( $\mu m$ )
Xfmr	$L_{pri}$ 1.047 nH, $L_{sec}$ 388.3 pH	250 x 250
$L_1$	3.316 nH	100
$L_g$	747.9 pH	80
$L_s$	173 pH	60
$L_l$	985.3 pH	60 x 60
$C_1$	58.6 fF	7.8 x 7.8
$C_p$	263 fF	16.3 x 16.3
$C_{var}$	3.33 pF nominal	38.5 x 47.4
$C_C$	3.70 pF	20x20
$R_g$	75 $\Omega$	19.2 x 5.6
$R_l$	123.7 $\Omega$	16.6 x 2.5
$R_B$	10 K $\Omega$	1.6 x 5.5

formance are  $f_T$  and  $f_{max}$ . The maximum speed at which a transistor can operate is defined by the unity gain frequency,  $f_T$ , and the maximum frequency,  $f_{max}$ , of the device.  $f_T$  is defined as the frequency at which the current gain, shown in Equation 4.27, of the device is equal to one.

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (4.27)$$

$f_{max}$  is the maximum frequency at which power gain is achieved and is equal to one [35] as shown in Equation 4.28.

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi R_{gg} C_{gd}}} \quad (4.28)$$

Large MOSFET width (W) is required to obtain high value of  $g_m$  and to increase the  $f_T$  and  $f_{max}$  frequencies. The large  $g_m$  improves gain and also reduces noise, as the minimum noise figure of a MOSFET is inversely proportional to the  $g_m$  as shown in Equation 4.29 [36], where  $R_{gg}$  is the gate resistance,  $K_2$  is the constant and  $R_s$  is the

**Table 4.2** Active Device Parameters

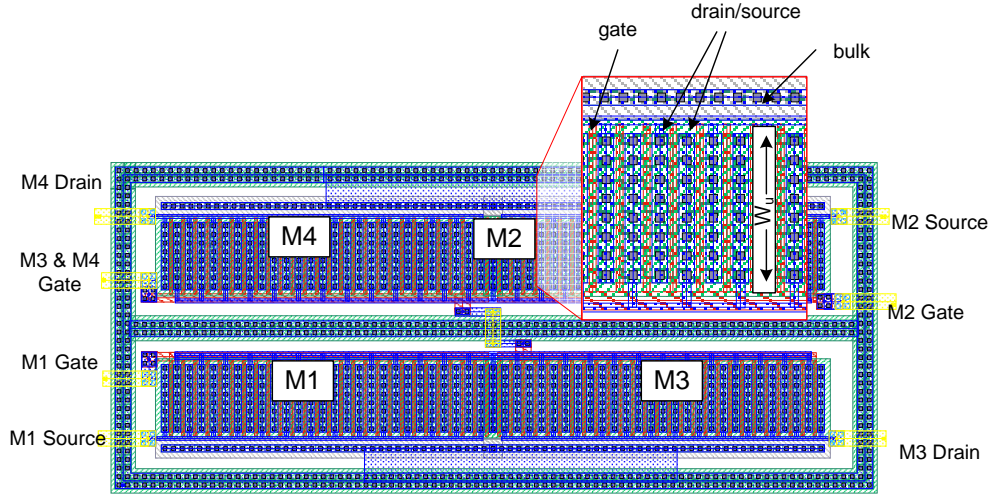
MOSFET	Width ( $\mu m$ )	Length ( $nm$ )	Unit Width ( $\mu m$ )	Fingers
$M_1$	108	180	4	27
$M_2$	108	180	4	27
$M_3$	108	180	4	27
$M_4$	108	180	4	27
$M_5$	64	180	4	16
$M_6$	80	180	4	20
$M_7$	3	180	1	3
$M_8$	600	180	15	40
$M_9$	750	180	15	50
$M_{10}$	632	180	8	79
$M_{11}$	592	180	8	74
$M_{12}$	400	180	25	16
$M_{13}$	400	180	25	16
$M_{14}$	32	360	4	8

source resistance.

$$F_{min} = 1 + K_2 C_{gs} \sqrt{\frac{(R_{gg} + R_s)}{g_m}} \quad (4.29)$$

The disadvantage of large  $W$  is that the gate resistance,  $R_{gg}$ , also increases. As  $R_{gg}$  becomes large,  $f_{max}$  will decrease and the minimum noise figure will increase. To reduce  $R_{gg}$ , and at the same time, keeping  $g_m$  large, the MOSFET width is broken down in smaller unit width ( $W_u$ ) and connected in parallel. The number of  $W_u$  in parallel is known as gate fingers. The width of a MOSFET is effectively equal to the number of gate finger multiplied by the unit width  $W_u$ . This implementation allows for the realization of larger width MOSFET without increasing  $R_{gg}$ . In the design, a minimum length of  $0.18 \mu m$  was used to keep  $g_m$  and  $f_t$  high. The only exception is the  $M_{14}$  length which defined the Q tuning voltage range. The MOSFET design parameters for the filter are shown in Table 4.2.

Another advantage of implementing large MOSFET using multiple fingers is that it allows the laid out of the transistor to be smaller and compact to better utilize chip area. The size of the MOSFET can be reduced by the sharing of the drain and

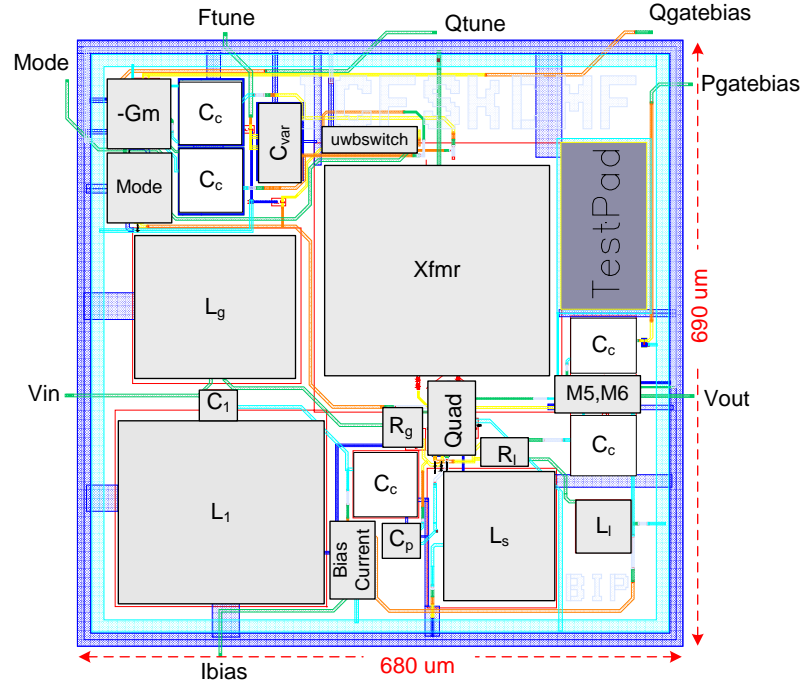


**Figure 4.16** A Layout of M1, M2, M3 and M4 MOSFETs

source nodes between fingers and MOSFETs. Shown in Figure 4.16 is a layout of the MOSFETs M1, M2, M3 and M4. The drain of one transistor is used as a source for another. The tight layout of the MOSFETs allowed for tight matching between unit fingers.

#### 4.3.5 Filter Chip Layout

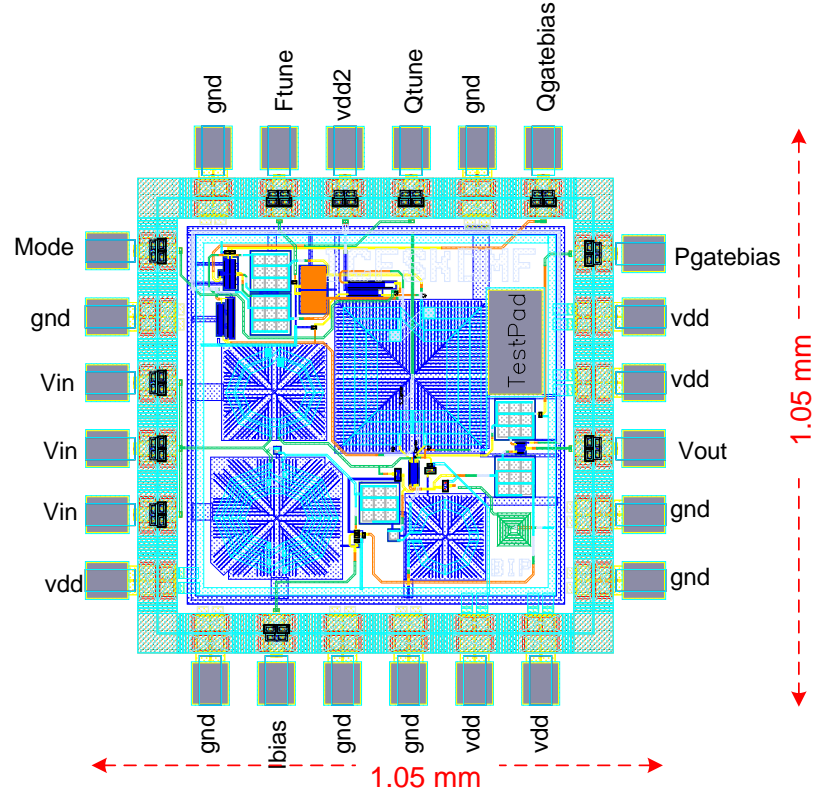
The floor plan of the filter including power and ground rings is shown in Figure 4.17. The filter occupies a die dimension of  $680 \mu m$  by  $690 \mu m$ . Detailed layout designs for the passive devices including resistor, capacitor, varactor, inductor and the transformer can be found in Chapter 3. The other blocks in the diagram shows the group of transistors making up the building blocks of the filter. M8 and M9 makes up the Mode block. The -Gm block consists of M12, M13 and M14. M10 and M11 makes up the *uwbswitch* block. The Quad block consists of the LNA transistors M1-M4. M5 and M6 are the second stage block. The Bias Current block consists of M7 and the RF blocker resistors.



**Figure 4.17** Die Floor Plan

To minimize the usage of I/O pins, the gate of M3 and M4 are internally biased at 1.4 V using polysilicon resistors. For debugging purposes, a test pad is added to allow direct probing of the gate voltage. The I/O ports consist of *Mode*, *Ftune*, *Qtune*, *Qgatebias* (*Vbias2*), *Ibias*, *Vin* and *Vout*. External biasing can compensate for process and environmental variations allowing more control during testing. Power ring and metal ring are placed at the outer edge of the chip to provide the shortest connection distances to the blocks.

The chip I/O are made via  $65\ \mu\text{m} \times 75\ \mu\text{m}$  pads which also provide electrostatic discharge (ESD) protection. The complete die layout with pads occupy an area of  $1.05\ \mu\text{m}^2$  as shown in Figure 4.18. Sufficient number of *vdd* and *gnd* pads placed sparingly around the chip limits the effect of IR-drop and other power-related issues. More *vdd* and *gnd* pads will limit the parasitic inductance effect of the bond wires on the filter. The inductance in the bond wire makes input impedance matching difficult



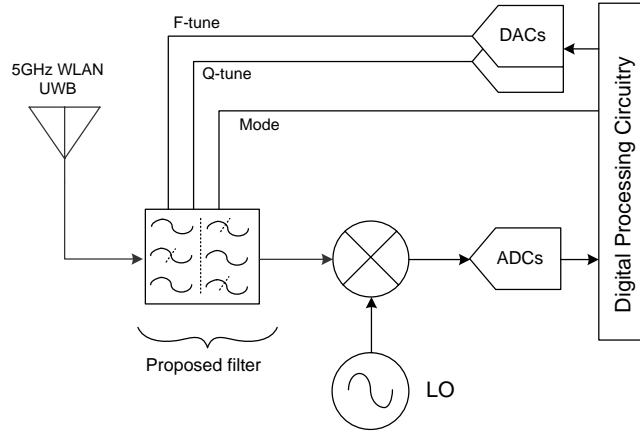
**Figure 4.18** Die Layout With Padding 1.05 mm x 1.05 mm

as the model is inaccurate. To reduce the effect of bond wires, The  $V_{in}$  pads are connected in parallel to three bond wires. Placement of  $V_{in}$  and  $V_{out}$  pads at the middle allows for the shortest bond wire length to package connection minimizing the resistance and inductance effects.

#### 4.3.6 A Receiver Architecture for the Proposed Filter

The dual mode Q-enhanced filter proposed in this work can be used in a receiver architecture as shown in Figure 4.19. The sub-sampling receiver [37] utilizes Q-enhancement filtering at RF frequencies and a down conversion mixer followed by conversion to a digital IF frequency using an ADC. Frequency tuning and Q adjustment are to be digitally controlled via the DACs. The dual mode filter can receive

either 802.11a (5 GHz WLAN) or UWB depending on the voltage at *Mode*. The digital processing circuitry is used for demodulation and assuming it has a NB interference block to detect and track the NB interference.



**Figure 4.19** Direct Subs-Sampling Receiver Architecture

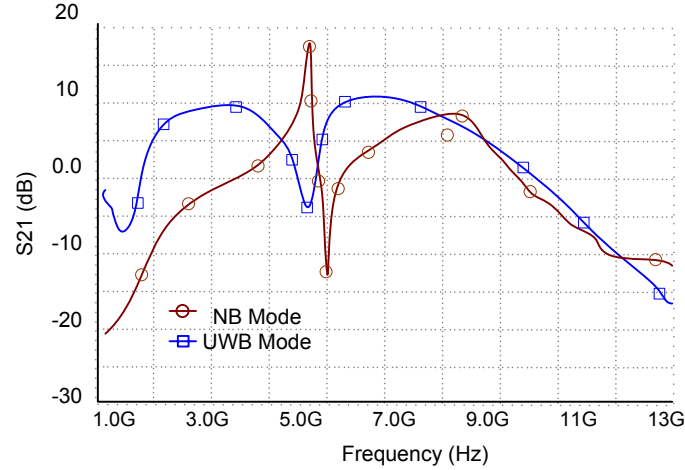
## 4.4 Simulation Verification

In the simulations, parasitic affects from bond wires and bond pads were included in the test bench. Since physical extraction of inductor and transformer passive devices were not possible, their compact models accurate at 5 GHz were used. The rest of the filter components were extracted for parasitic effects from the layout to account for unwanted coupling, noise and device mismatch. The following simulations were used to verify the performance of the filter both in the NB and the UWB modes.

### 4.4.1 NB and UWB Filter Response

The responses of the filter in the NB and UWB mode are plotted in Figure 4.20. The filter has a gain, in NB mode, of 15 dB at the resonance frequency of 5.3 GHz. A secondary peak can be observed at approximately 8 GHz. This is caused by the

resonance of the interwinding parasitic capacitance with the primary winding of the transformer. As the resonance is outside of the 5 GHz pass band, the parasitic gain is not important. In the UWB mode, the filter operates as a wideband LNA with a

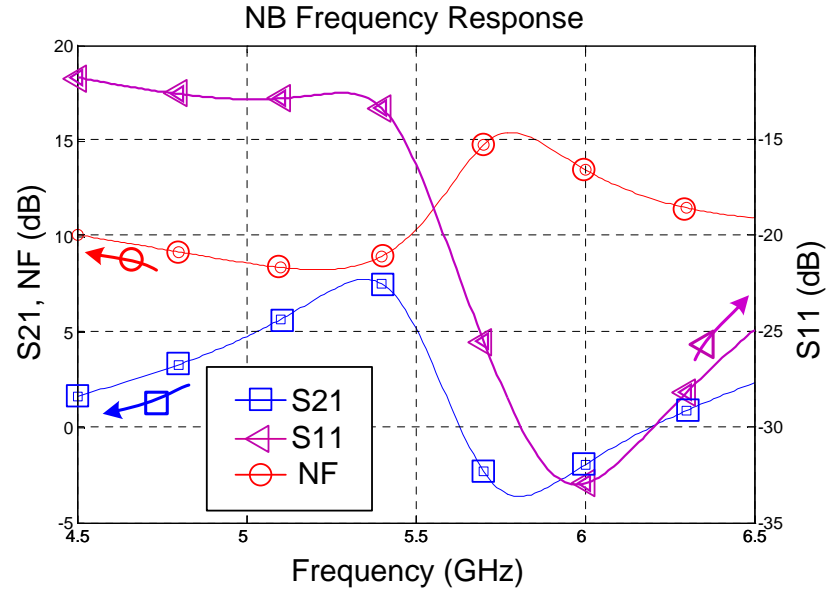


**Figure 4.20** Filter Response in NB and UWB Mode

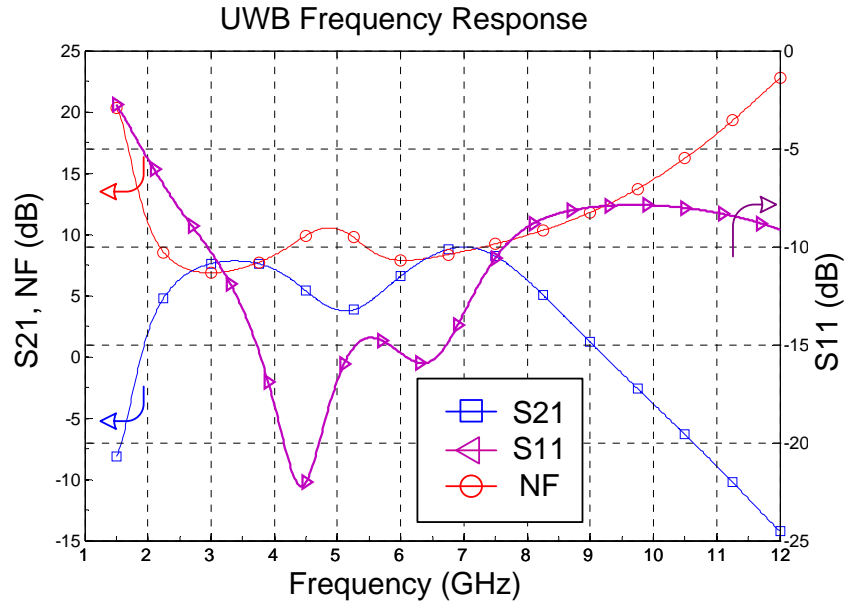
tunable notch filtering at 5 GHz. The wideband gain is observed from 1.8 GHz and gradually deviates to zero at 9 GHz. The low gain at high frequency is mainly caused by the parasitic capacitances of M5 and M6 in the second stage of the filter. A notch response created by the Q-enhancement resonator can be seen at 5.3 GHz.

Figure 4.21 shows the S11, S21 and NF responses of the filter in the NB mode. At a peak gain of 8 dB, the input impedance matching is -13 dB and NF is 8 dB. Figure 4.22 shows the frequency response of the filter in UWB mode with the notch resonator off. The filter acts as a LNA from 2 GHz to 9 GHz. A small dip is observed at 5 GHz due to the minimal effect of the resonance circuit. From 3.1 GHz to 10.6 GHz, the input impedance is matched to better than -7.5 dB. The NF of the filter varies across the operating frequencies. From 3 GHz to 8 GHz, the NF is less than 10 dB. At 5 GHz, the NF increases as the interference rejection power increases. NF deteriorates after 8 GHz due to the drop in gain.

The main source of the noise contribution occurs from the NB and UWB fil-



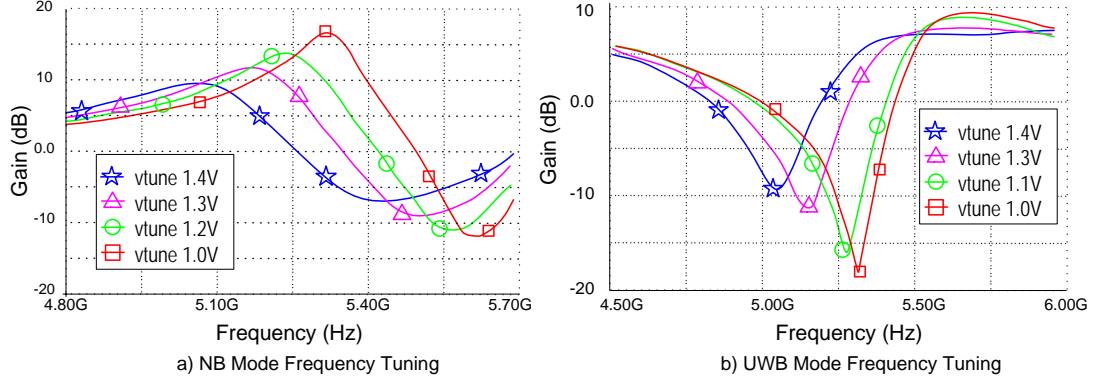
**Figure 4.21** NB Gain (S21), Input Matching (S11) and NF Characteristics



**Figure 4.22** UWB Gain (S21), Input Matching (S11) and NF Characteristics

ter sharing the same input resulting in input power loss. The other source is from the matching network and from noise injected by the Q-enhanced resonator via the





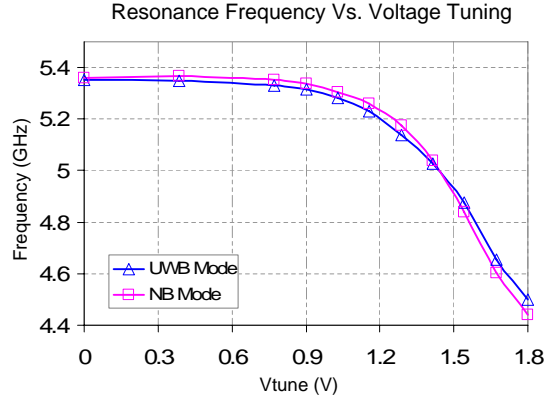
**Figure 4.23** NB and UWB Mode Frequency Tuning for Fixed Q-tune Voltage

transformer.

#### 4.4.2 Filter Tuning

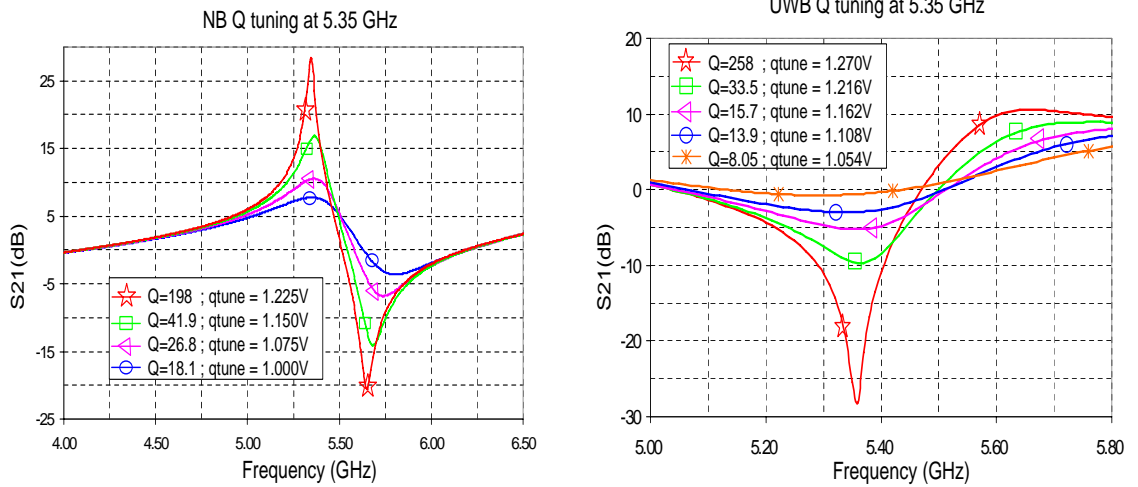
Filter tuning is verified by varying the voltage, *vtune*, across the varactor and observing the response of the filter. The responses of the filter in NB and UWB modes are plotted in Figure 4.23. When *vtune* is at 1.0 V, the resonating frequency is at located 5.35 GHz. As the voltage increases, the varactor capacitance increases resulting in a lower resonating frequency. The graph shows that the filter has a tuning range from 5 GHz up to 5.35 GHz. The same tuning reference voltage, used for tuning both modes, as shown confirmed in Figure 4.24. The two curves show that the notch and bandpass response corresponds to the same tuning voltage.

The Q-tuning voltage, *qtune*, controls how much current flows through the transistor, M14, which dictates the degree of negative impedance compensation. As *vtune* increases,  $g_m$  increases, resulting in higher Q as shown in Figure 4.25 for NB and UWB modes. As the resonance frequency decreases, the amplitude of the filter gain or rejection decreases. As the varactor capacitance increases, the varactor Q decreases resulting in the effective Q of the resonator to drop. Compensation is made by increasing the negative resistance of the resonator by increasing the *qtune* voltage



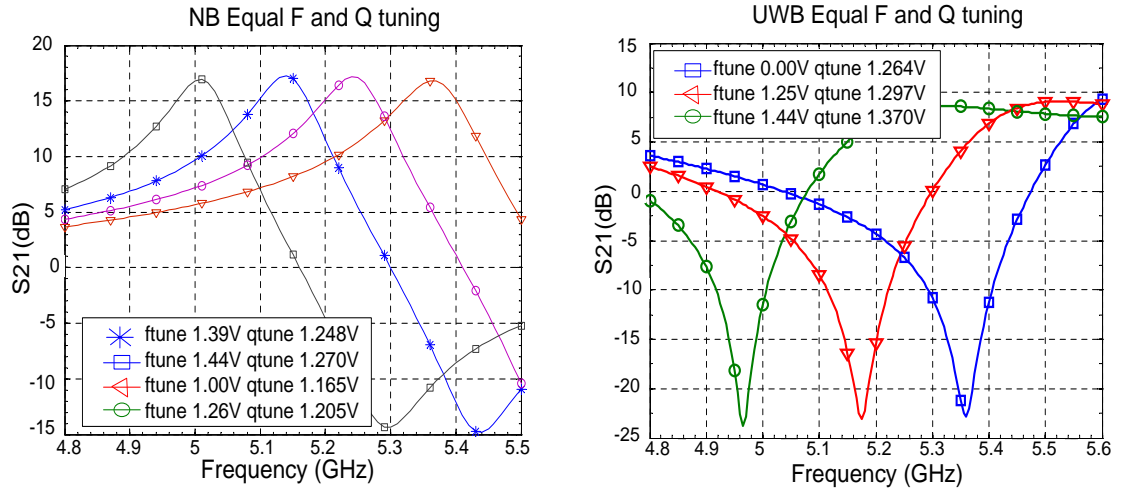
**Figure 4.24** Location of Resonance Frequency Vs. Tuning Voltage for NB & UWB mode

as shown in Figure 4.26(a) in the NB mode and Figure 4.26(b) in the UWB mode. Figure 4.26(a) shows Q compensation is used to make the gain of the filter constant across all frequencies. As  $vtune$  increases, the Q of the varactor decreases requiring  $g_m$  to be larger to compensate.



(a) NB Filter Q increases as voltage increases (b) UWB Filter Q increases as voltage increases

**Figure 4.25** Q-tuning for the NB and the UWB Modes



(a) Uniform NB tuning by varying both F and Q (b) Uniform UWB rejection tuning by varying both F and Q voltage

**Figure 4.26** Equal Amplitude Frequency Tuning By Varying Q for NB and UWB Mode

### 4.4.3 Filter Stability

Two criteria must be met for the filter to be unconditionally stabled [38].  $K$  is the Rollett stability factor and  $B_1$  is the 2-port stability criterion as given by,

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (4.30)$$

where  $\Delta$  is the determinant of the S-parameter matrix.

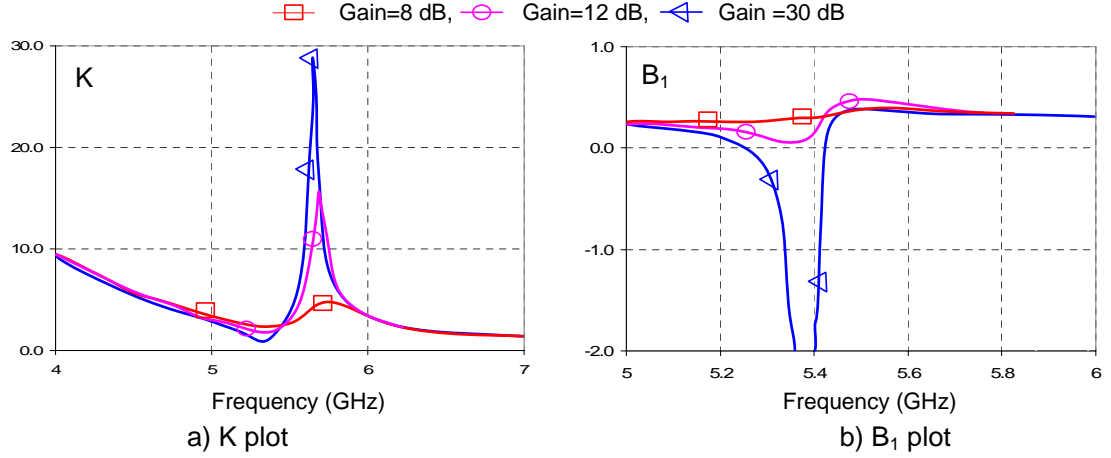
A set of necessary and sufficient conditions for unconditional stability are:

$$K > 1 \quad (4.31)$$

$$B_1 > 0 \quad (4.32)$$

Figure 4.27 shows the  $K$  and  $B_1$  parameters of the filter in NB mode. As Q increases, gain increases until the filter becomes unstable.  $K$  indicates instability when the gain is more than 21 dB.  $K$  equals to 0 at a gain of 30.  $B_1$  is approximately equal to .33 at the passband when gain is less than 12 dB. As gain increases above

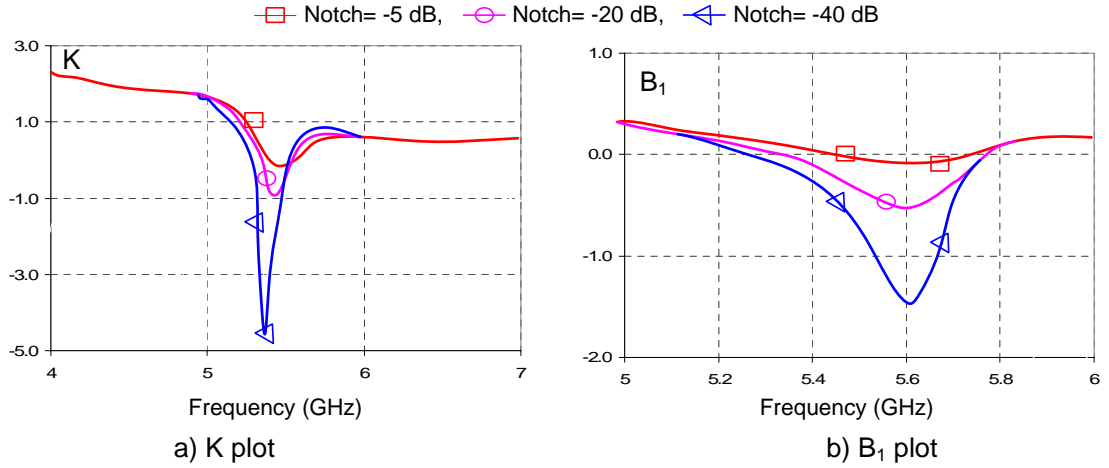
18 dB,  $B_1$  drops below 0 indicating instability.



**Figure 4.27** Stability Plot in NB Mode a) K Plot b)  $B_1$  Plot

Inductive degeneration can generate positive resistance looking into the gate of a MOSFET while capacitive degeneration generates negative resistance. Negative resistance can lead to instability of the filter [39]. In the UWB mode, the transformer is used to provide notching through the degeneration inductor. However, at frequencies below the notch frequency, the input resistance appears positive. At frequencies above the notch frequency, it will appear negative which can lead to instability. Figure 4.28 shows the  $K$  and  $B_1$  plot for the UWB filter. At passband frequencies below the notch,  $K > 1$  and  $B_1 > 0$  so it is unconditionally stable. At frequencies above the notch,  $K < 1$  and  $B_1 > 0$  which means conditions can lead to instability.

To prevent the filter from being unstable at the passband at 5 GHz, oscillation must be avoided. This occurs when the loss in the primary winding is over compensated. Care must be taken not to over-compensate for the losses in the filter to prevent instability.



**Figure 4.28** Stability Plot in UWB Mode a) K b)  $B_1$

#### 4.4.4 Linearity

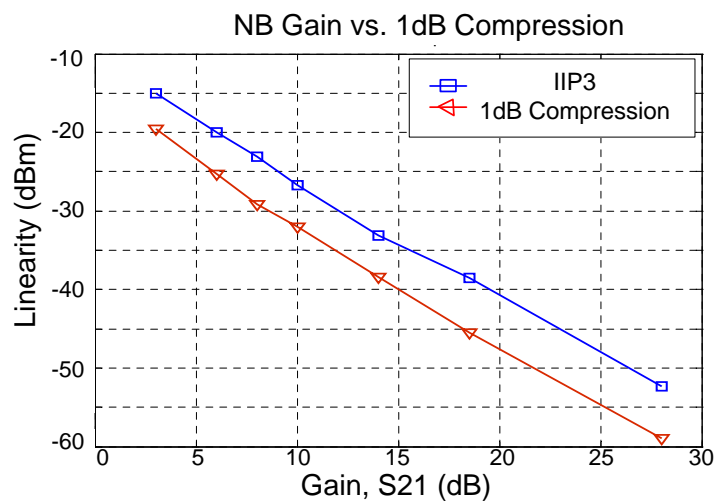
Linearity defines the upper bound of the signal strength and needs to be high to satisfy the high dynamic range requirement of a receiver. Equation 4.33 states that the relationship between dynamic range is inversely proportional to the Q of the filter.  $Q_o$  is the non-enhanced Q of the filter, whereas,  $Q_{enh}$  is the new enhanced filter Q.

$$DR \propto \frac{1}{Q_o Q_{enh}^2} \quad (4.33)$$

Using a lower  $Q_o$  tank can actually improve the dynamic range of the Q-enhanced filter up to the point where the noise of the enhancement filter starts to dominate [40]. As the Q of the filter is enhanced, dynamic range is reduced as linearity decreases.

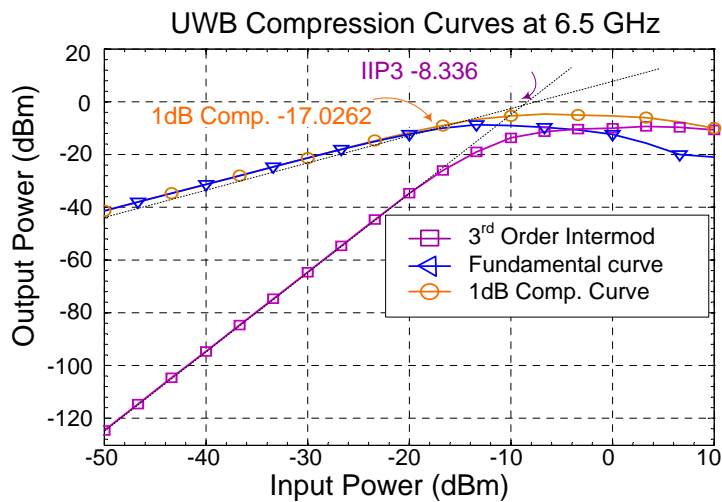
In the NB mode, the gain of the filter is tunable by the Q-enhancement resonator, linearity of the filter is also adjustable as it is inversely dependent on the gain. Figure 4.29 shows the effect of Q-enhancement in the NB mode. The plot shows the inverse relationship between linearity and gain as plotted by the 1-dB compression point and the input referred IP3 point.

In the UWB mode, the linearity points are taken at 6 GHz where the filter gain



**Figure 4.29** 1dB and IIP3 Compression Point Vs. Gain

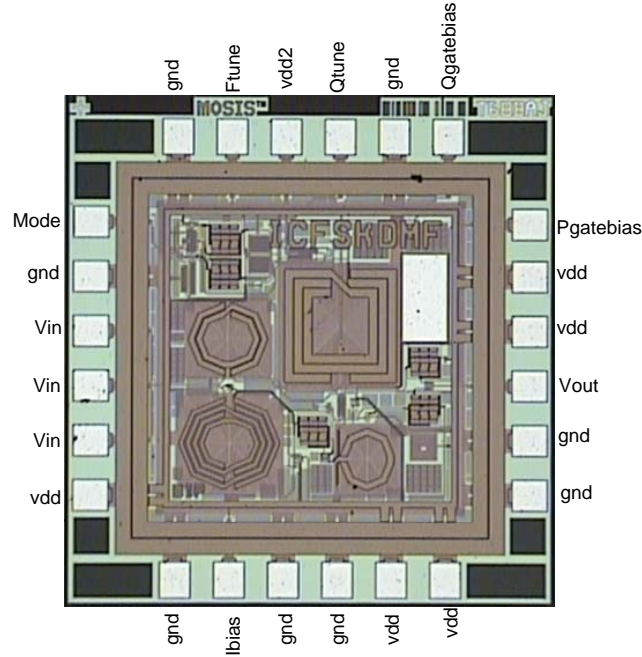
peaks at approximately 8 dB. Shown in Figure 4.30, the filter has a 1-dB compression point of -17 dBm. The input IP3 point of -8.3 dBm is simulated with two signals located at 6 GHz and 6.1 GHz



**Figure 4.30** 1dB and IIP3 Compression Plot for UWB at 6.5 GHz

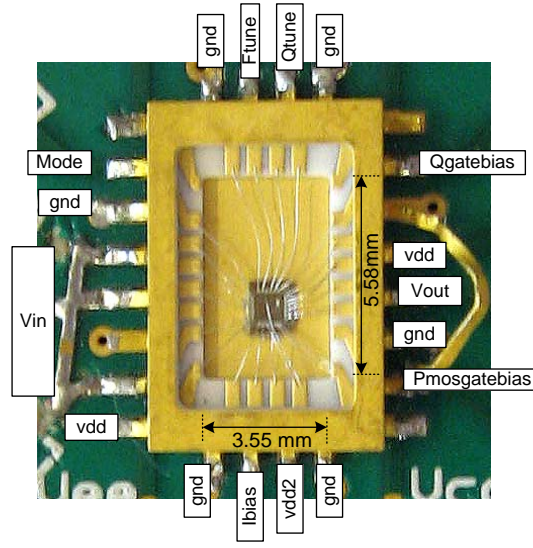
## 4.5 Measurement Verification

The micrograph of the dual mode filter fabricated using a  $0.18\mu m$  CMOS process is shown in Figure 4.31. The die occupies an area of  $1.1\text{ }\mu m^2$  and containing six bond pads on each side.



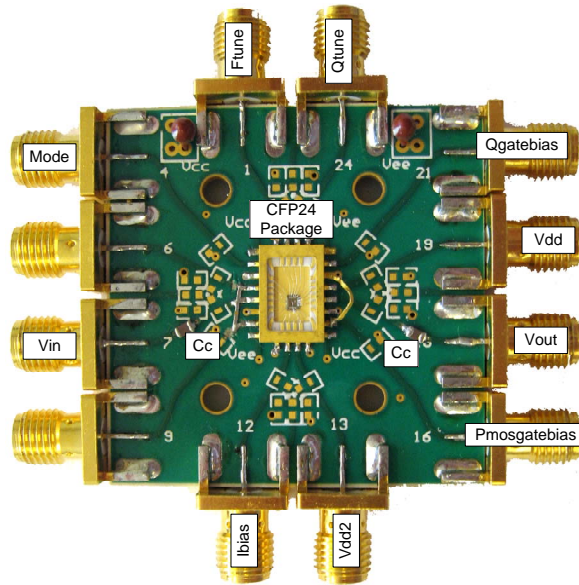
**Figure 4.31** Filter on  $0.18\text{ }\mu m$  CMOS  $1.05\text{ mm} \times 1.05\text{ mm}$  Die

Packaging and fixturing are needed to interface with the RF testing equipments to measure the performance of the chip. Due to the unavailability of high RF packaging and fixturing available, the 24 pin CFP package and fixture are used. The chip is packaged in a 24 pin CFP package with a cavity dimension of  $3.55\text{ mm}$  by  $5.58\text{ mm}$  as shown in Figure 4.32. The small cavity size of the package allows for shorter bond wires to be used. The *Pmosgatebias* pin is soldered to another pin for easier access to the test fixture SMA port. The CFP package was soldered to the PCB test fixture as shown in Figure 4.33. The fixture is connected to the external test environment via SMA connectors located at various locations around the board. The signal paths



**Figure 4.32** Chip on 24-CFP Packaging

from the package to the SMA connectors are through  $50\ \Omega$  controlled impedance lines. All ground I/O are connected to a ground plane. Ten SMA ports provide access for testing. Coupling capacitor,  $C_c$ , of  $1\text{ nF}$  was added at the RF input and output.



**Figure 4.33** CFP-24 Test Fixture

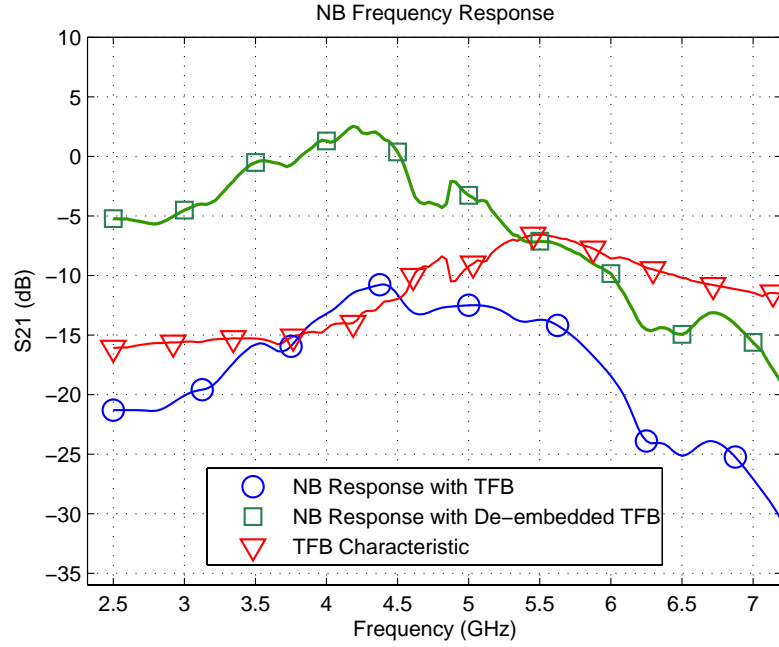


The 24-CFP package and test fixture are designed for circuits with frequencies of up to 4 GHz, but should give an idea of the response of the dual mode filter. High frequency packaging and test fixture board operating over 10 GHz is required to fully characterize the filter without resulting any significant performance degradation caused by the packaging and test fixture. The addition of the 24-CFP package causes signal degradation due to excessive insertion loss and insufficient return loss as it was not accounted for in the design.

### 4.5.1 Filter Gain Measurement

#### NB Gain

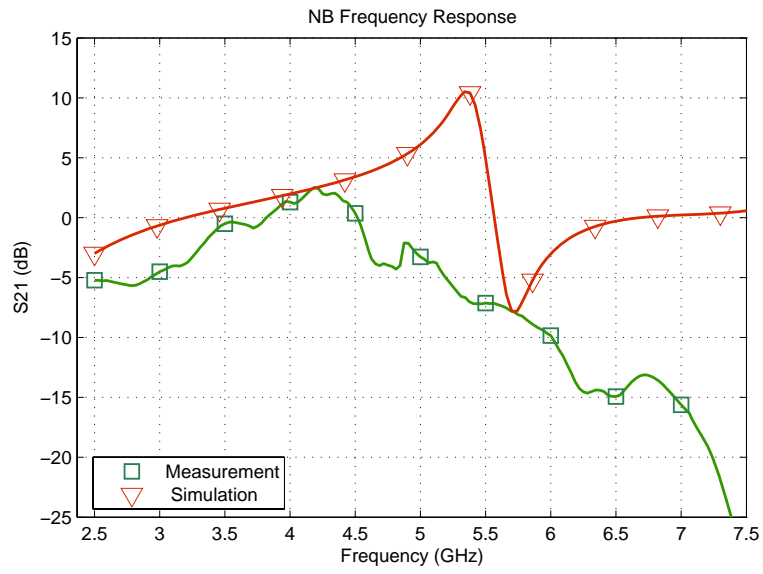
RF performance degradation can be contributed by the losses in low performance interconnects and parasitics in the pads. The majority of the loss are associated with the coupling from signal pads to ground pads that originate from the pad/substrate capacitance and the semi-conducting nature of the silicon substrate [41]. Since the model of the 24 CFP package was not available, its parasitic effects could not be isolated from the filter. However, the parasitics from the test fixture were isolated by using a  $50\ \Omega$  impedance line to short the input and output pins and characterizing the board. The response of the test fixture board and the filter are shown in Figure 4.34. The filter has a gain less than 0 dB across all frequencies when the test fixture was included in the measurement. However, when the test fixture was isolated from the filter, the filter gain starts to appear above 0 dB as shown with the  $\square$  curve. The filter has a peak gain of 2.5 dB at 4.2 GHz. Figure 4.35 shows a comparison between the measured bandpass response and the simulated response. From 2.5 GHz to approximately 4.3 GHz, the measurement corresponds to the simulations with about 1-3 dB loss due to the package and bond wires. For frequencies above 4.3 GHz, the filter gain degrades as the parasitics from the package and test fixture board begins to dominate. The results confirm that the standard 24-CFP package and test fixture board are not suitable for use in RF circuits operating above 4 GHz frequency.



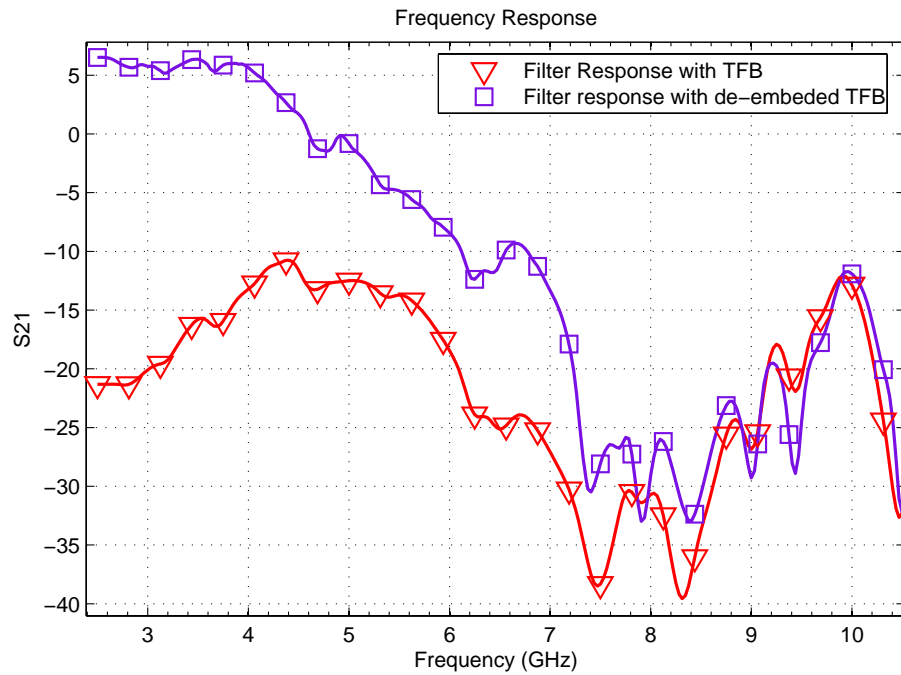
**Figure 4.34** NB Gain ( $S_{21}$ ) Response with TFB and with de-embedded TFB

## UWB Gain

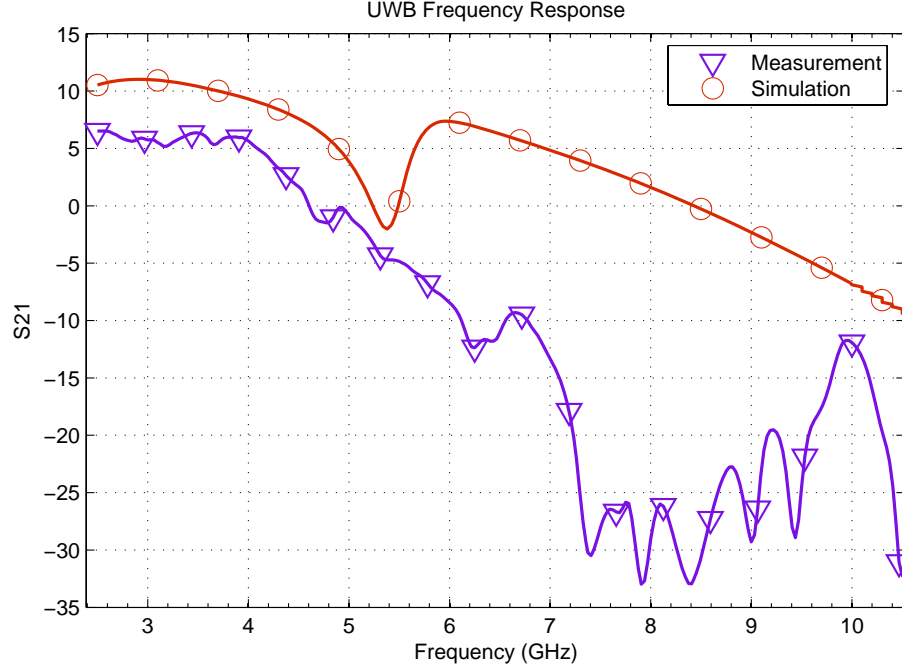
The gain response measurement of the filter in UWB mode is plotted in Figure 4.36. The two curves show the filter response before and after the de-embedding of the test fixture board. As can be seen, the board has a drastic effect on the filter's performance. Similar to the observation in the NB mode, after approximately 4 GHz, the response of the filter drops below 0 dB due to the parasitics in the packaging. Comparison of the measured and simulated results are shown in Figure 4.37. As expected, the measured gain is 3-4 dB lower than the simulated gain up to until 4.5 GHz. Above this frequency, the losses are too much to measure the filter's response. The filter is designed with a notch at 5 GHz, however the notch appears to be located around 8 GHz when measured.



**Figure 4.35** NB Gain Simulation Vs. Measurement



**Figure 4.36** UWB Gain (S21) Measurements



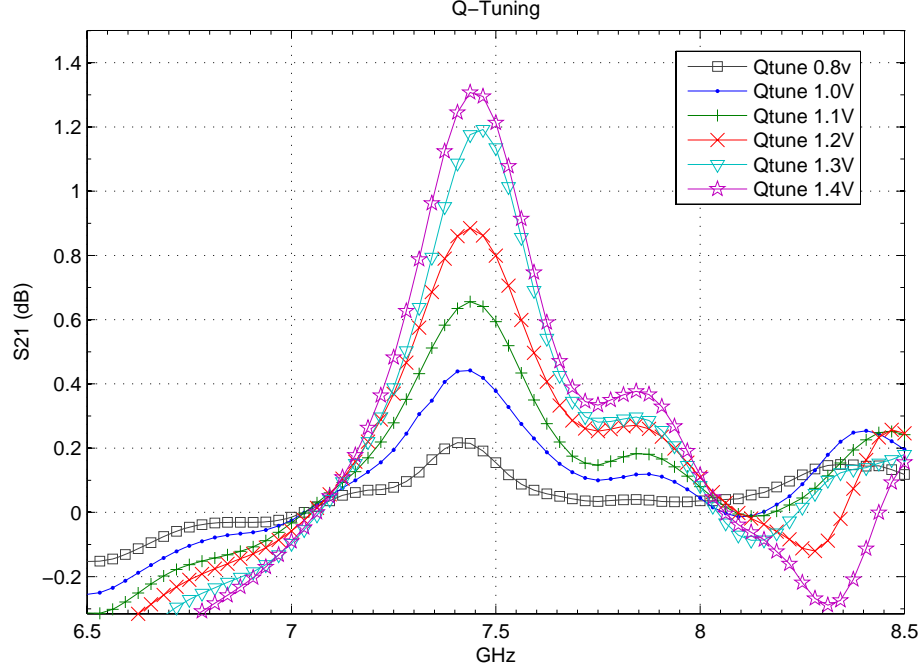
**Figure 4.37** UWB Gain (S21) Simulation Vs. Measurement

## Filter Tuning

The Q-enhancement measurement of the filter in NB mode is shown in Figure 4.38. As the Qtune voltage is increased gradually from 0.8 V to 1.4 V, the gain varies from 0.2 dB to 1.3 dB. Hence, the measurement confirms that the resonance frequency is located around 7.5 GHz and not at 5 GHz as simulated. The gain is also very small indicating that there are very little mutual coupling between the primary and secondary windings of the transformer.

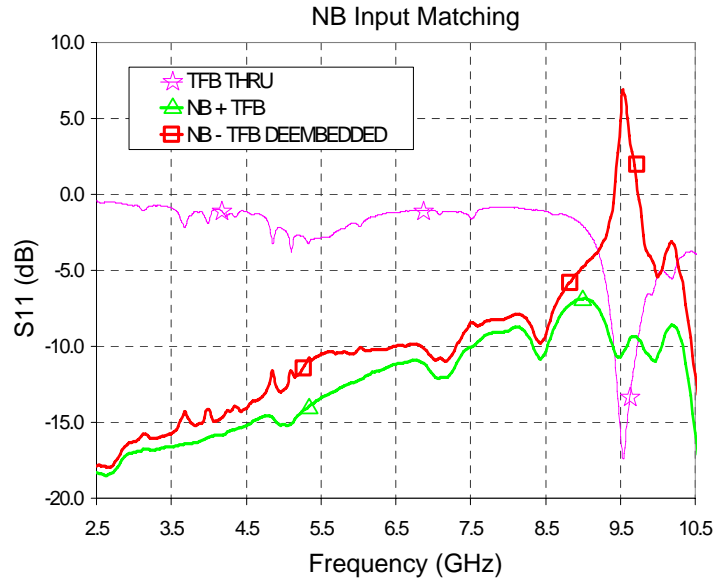
## 4.5.2 Impedance Matching Measurement

Transmission line effects cause phase shift and losses resulting in an incorrect matching, which are dominant at high frequencies. Figure 4.39 shows the S11 plot of the filter in NB mode. The curves represent the response of the filter with and without the effect of the test fixture board. The insertion loss after de-embedding is

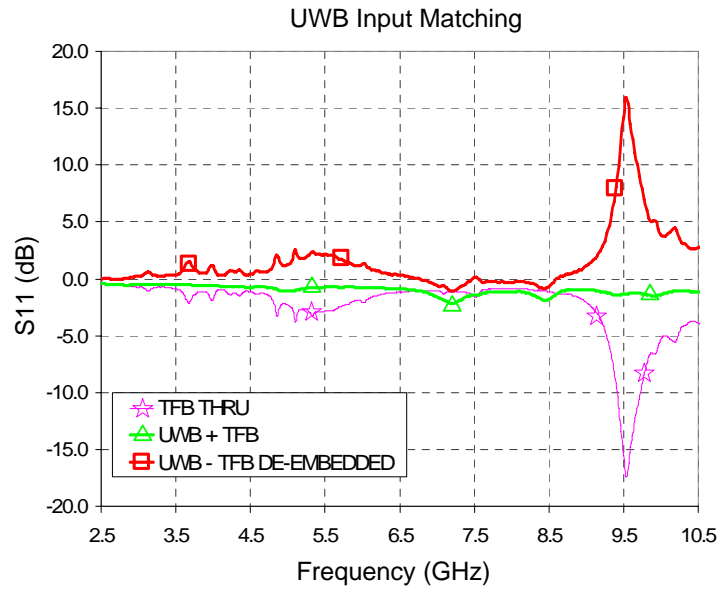


**Figure 4.38** Q Tuning in NB Mode Responds at 7.5 GHz

approximately -11 dB at 5.35 GHz. Variations between simulations and measurements are mainly due to the package and test fixture and mismatch at the input and output due to transmission line effect. Figure 4.40 shows the input impedance matching for the filter in UWB mode. The plot shows that impedance matching is poor and not enough power is transferred to the filter. The input impedance matching of the two filters can be corrected by using off-chip filtering to take into account of the parasitic effects and transmission line in the packaging and test fixture board. The plots verify that the insertion loss is significant, particularly at higher frequencies. NF was not measure as it is highly dependent on the quality of the input matching.



**Figure 4.39** Input Impedance (S11) Plot for NB



**Figure 4.40** Input Impedance (S11) Plot for UWB

## 4.6 Measurement Summary

Designing RF integrated circuits that require packaging and test fixturing presents many challenges. Due to the limitation of packaging and test fixture available during

the research, measurements were only confirmed up to 4 GHz. After 4 GHz, the mutual inductance between bond wires effectively increase the inductances effecting the input impedance matching and gain of the filter. The effects of signal coupling and parasitics in the packaging and test fixture board can dominate and degrade the filter response at high frequencies. Therefore, packaging selection and consideration in the early stage of the design is important. Package, PCB test fixture models and testing equipment must be readily available for RF high frequency designs. The choice of packaging method is also important. For high frequency circuits, more costly packaging such as flip-chip (gold-ball) can be used to eliminate the effects of the bonding wires.

## 4.7 Research Comparison

The measurements confirmed that the filter conforms to the expected characteristics of a bandpass filter while operating in NB mode and an LNA with notch filtering in UWB mode. However, due to the parasitic effects of bonding wires, the 24-CFP package and test fixture board, insertion losses and parasitic contributions were too significant to successfully validate the responses at high frequencies. Thus, the post simulation results shown in Table 4.3 will be used to compare with other recent works in RF front-end LNA and filters.

Ideal comparison of the dual mode filter to other works is difficult as there is no known dual-mode filters for both NB and UWB receivers. Several recent research work in UWB and NB LNA and Q-enhanced filters for the standard CMOS technologies are used to compare to the dual mode filter as shown in Table 4.4.

In [32], the UWB LNA achieves a gain of 9.3 dB, NF of 5.2 dB and input matching of -10 dB. However, the LNA does not include a notch filter yet occupies the same die area as the dual mode filter. In [42], the bandpass filter offers a low power and area design of 5.2 mW and  $0.05 \text{ mm}^2$ , respectively. To achieve low power, the filter

**Table 4.3** Filter Performance Post-Simulation Summary.

Parameter	NB Mode	UWB Mode*
Max. DC Current (mA)	13	13
Max. DC Power (mW)	23.4	23.4
Gain (dB)	4 - 25	0 - 8
NB Rejection (dB)	N/A	60
Noise Figure (dB)	8	$\leq 10$
1dB Comp. (dBm)	-55 to -23	-17
IIP3 (dBm)	-47 to -18	-8.3
Operating Bandwidth (GHz)	5.15 - 5.35	3.1 - 9
S11 (dB)	-16	$\leq -7$

\* Valid from 3 GHz to 9 GHz

**Table 4.4** Performance Comparison with Recent LNA and Filter Work

Parameters	2004 [32]	2002 [42]	2000 [43]	Dual Mode Filter	
Type	UWB LNA	NB Q-Enh. Bandpass	LNA with Rejection	NB Mode	UWB Mode
Technology	0.18 $\mu m$ CMOS	0.35 $\mu m$ CMOS	CMOS	0.18 $\mu m$ CMOS	0.18 $\mu m$ CMOS
Freq. (GHz)	3.1 - 10.6	2.1	1.88	5	3.1 - 9
Gain (dB)	9.3	10	24	4 - 25	0 - 8
Rejection (dB)	N/A	N/A	30	N/A	60
IIP3 (dBm)	-6.7	-18	-10	-47 - -18	-8.3
S11 (dB)	-10	N/A	N/A	-16	$\leq -7$
Avg. NF (dB)	5.2	26.8	5.5	8	10
Die Area ( $mm^2$ )	1.1	0.1	N/A	1.1	
Power Consumption (mW)	9	5.2	25.2	23.4	

does not have active gain. The design did not include an input matching network allowing the area to be minimized. But as a result, NF was poor at 26.8 dB. In [43], the authors designed a NB LNA with image rejection. It achieves a gain of 24 dB, NF of 5.5 dB and image rejection of 30 dB. The LNA does not include an input matching network, and the image rejection is not tunable. Power consumption is slightly higher than the dual mode filter at 25.2 mW.

In the design, the filter sacrifices several performances such as low linearity and



high NF to achieve dual mode functionality. The filter can operate as a Q-enhanced bandpass filter in NB mode and a LNA with tunable interference rejection in UWB mode. The filter is fully integrated occupying an area of  $1.1 \text{ mm}^2$  including the input impedance matching circuit. The gain and interference rejection are both tunable and consumes 23.4 mW of power.

## 5. Conclusions and Future Exploration

### 5.1 Conclusions

In this research, a dual mode Q-enhanced filter was developed with the following goals in mind: 1) to provide rejection at the presence of 802.11a interference in UWB mode. 2) to provide Q-enhanced bandpass filtering when operating in 5 GHz NB mode. A Q-enhanced transformer resonator coupled at the degeneration inductor of an LNA was used to provide notch interference rejection at 5 GHz followed by another amplifier to provide further gain from 3.1 GHz to 9 GHz. The same Q-enhanced transformer resonator was also coupled to the load of another LNA to provide channel selection to the bandpass filter in NB mode. The filter incorporates an NMOS and PMOS switch to turn on either bandpass or notch functionality depending on the mode of operation. The LC ladder matching network was modified with an addition of a resistor and inductor to enable a single-ended input matching for both NB and UWB.

The fully integrated filter occupies a small die area of  $1.1 \text{ mm}^2$  when I/O pads were added. Post layout simulations show a power consumption of 23.4 mW while achieving a gain of up to 25 dB and 8 dB for the NB mode and UWB mode, respectively. The filter is able to reject up to 60 dB of 5 GHz NB interference while operating as a UWB filter. Input impedance matching is better than -7 dB in UWB mode and -16 dB in NB. The noise figure in UWB mode is better than 10 dB from 3.1 GHz to 9 GHz and 8 dB at 5 GHz in NB mode.

The accomplishments achieved in this research are summarize as follow. A design of the first dual mode RF front-end filter for a NB and UWB receiver. A demonstra-

tion of a MOSFET switch operable at RF frequency for current control. A proposed modification to the LC Ladder matching network for simultaneous matching for narrowband and wideband. A design utilizing channel selection and notch filtering at the RF front-end to reduce receiver component count and complexity. Finally, a proposed idea of taking advantage of the co-existence between the 5 GHz WLAN and UWB to increase functionality in wireless devices.

## 5.2 Future Work

A dual mode filter topology taking advantage of the Q-enhancement technique was demonstrated to be applicable for NB and UWB receivers. Measurements show signal degradation at high frequencies due to the unavailability of high frequency packaging and test fixture. With better packaging and test fixture available, measurement results can be improved. Parasitic effects not associated with the filter can be eliminated by directly probing the die. Alternatively, high performance packaging such as flip-chip can be used to eliminate the parasitic inductance of the bond wires. Better results are to be expected when the filter is integrated with the rest of the front-end receiver blocks eliminating packaging requirement.

The design of the filter can be modified in several areas to improve the performances such as gain and noise figure. The effect of parasitic capacitance and resistance are amplified as the frequency of operation increases. As we found from our simulation results, the effect causes the gain of the filter in UWB mode to drop at 9 GHz. This was mainly due to the use of the active load in the second stage. However, it was necessary to reduce power and design a single output port for the filter. It was shown that the use of an inductor load can result in higher gain and noise improvement at high frequencies but requires more current to drive the M5 and M6 separately [34].

The goal of the dual mode filter design is aim at minimizing area for low cost. Hence, it was designed such that both UWB and NB applications share the same

input and output. Although this improves integration with the antenna and receiver, the setback is higher noise figure and less than optimal input matching for both NB and UWB. A modification to the design is to isolate the NB and UWB input. This allows for separate NB and UWB impedance matching network allowing for minimal insertion losses. These changes will bring better performance to the filter while trading off die area and power.

Future work on the research can also be expanded to redesigning the transformer using advanced 3D simulation tools. As shown from the simulation and measurement, the six port center-tapped model did not accurately model the transformer response as it did not account for interwinding couplings. To reduce complexity, two 4-port transformers can be implemented instead of a center-tapped transformer to isolate the coupling. 3D simulation tools such as EM or FastHenry will aid with the accuracy that is required for advanced Q-enhanced transformer filter design.

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